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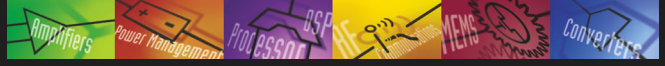

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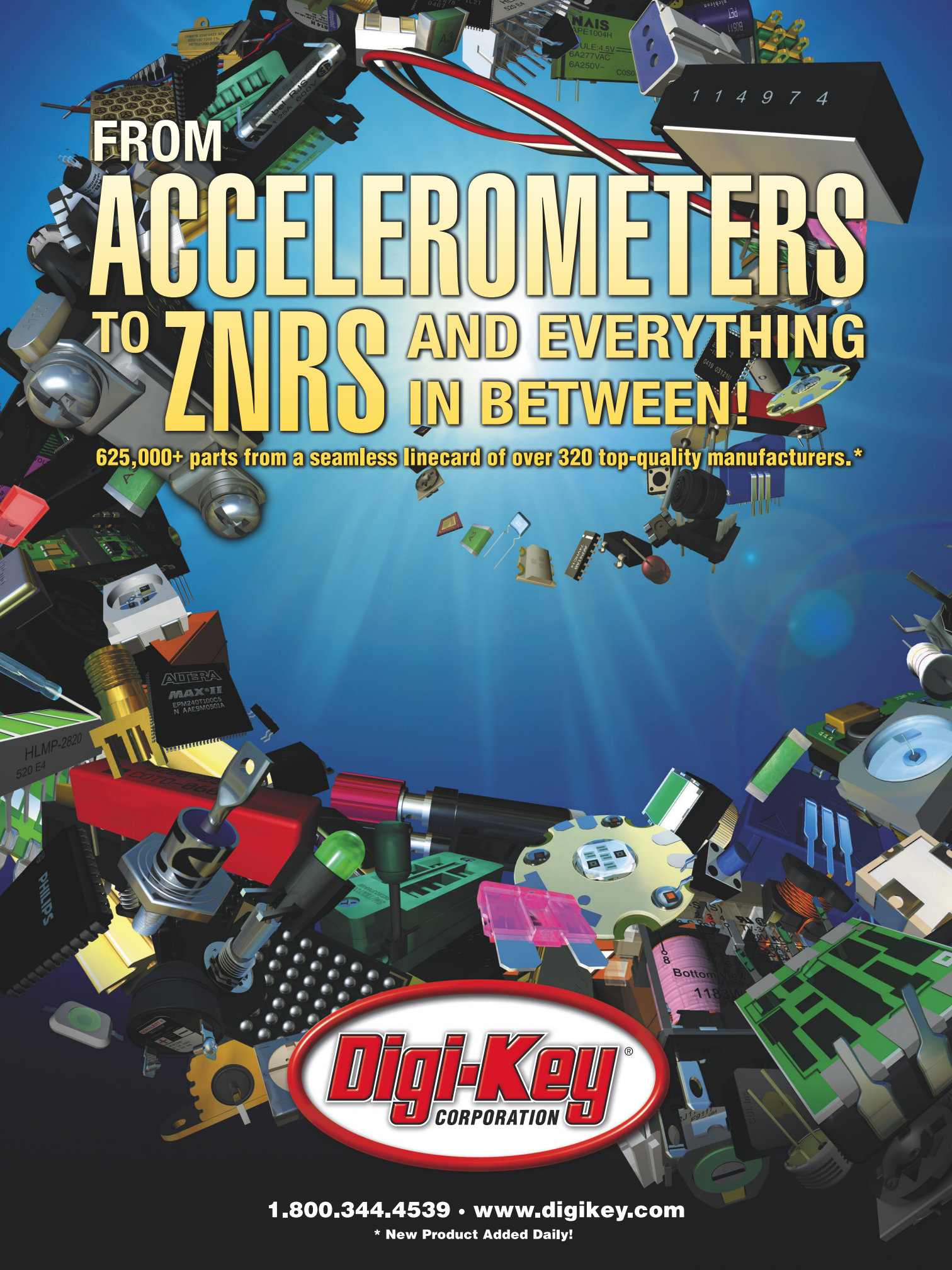
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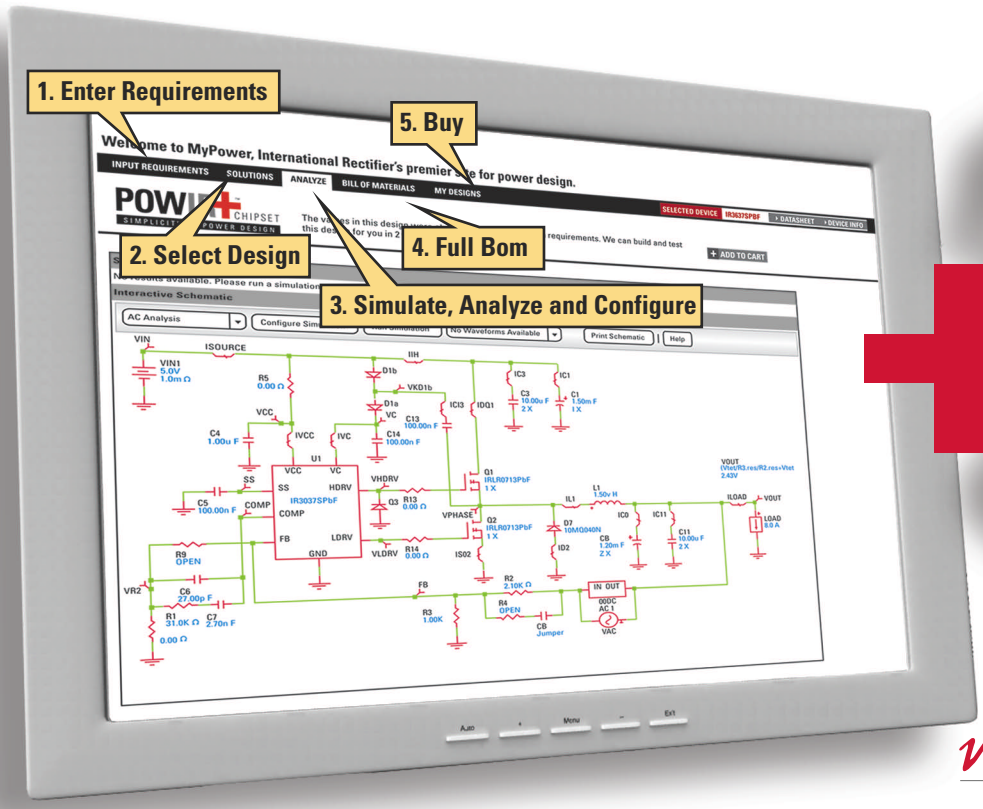

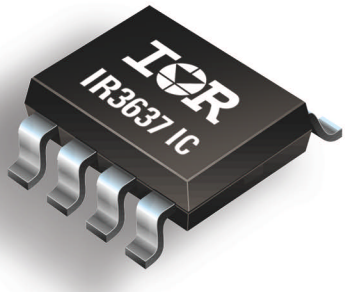

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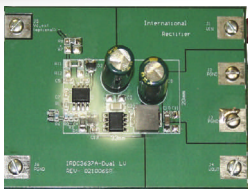
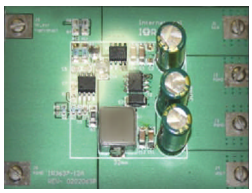
IRPP3637-06A



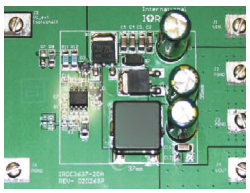
$5V_{in}$ / $1.25V_{out}$
@ 6A & 600kHz ~1.0in²

IRPP3637-12A



$12V_{in}$ / $1.8V_{out}$
@ 12A & 400kHz ~1.5in²

IRPP3637-18A



$12V_{in}$ / $3.3V_{out}$
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IRPP3637-12A	12V	1.8V	12A	400kHz	IR3637S, IRF7823, IRF7832Z		
IRPP3637-18A	12V	3.3V	18A	400kHz	IR3637S, IRLR8713, IRLR7843		
IRPP3637-06AC	3.0V to 13.2V	0.8V to 5.0V	Up to 6A	400kHz or 600kHz	Various	1-2 Wks	Customizable Ref Design BOM configurable on-line. Operating range defined is NOT possible with one BOM
IRPP3637-12AC			Up to 12A		Various		
IRPP3637-18AC			Up to 18A		Various		

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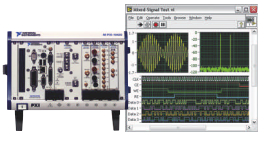

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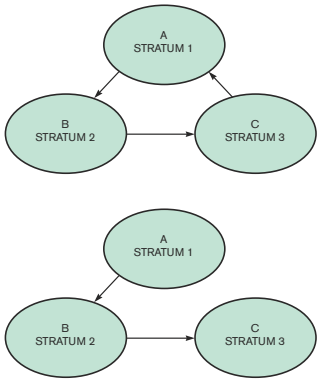
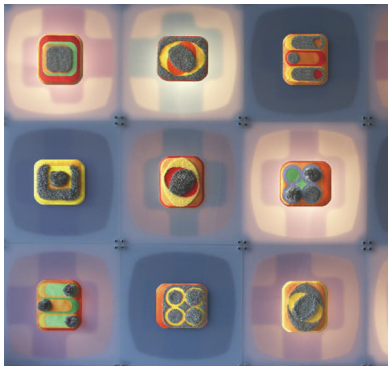


The 33rd Annual Microprocessor Directory:

Nontrivial pursuit



Fabrics get smart

Accurate clocks optimize network service

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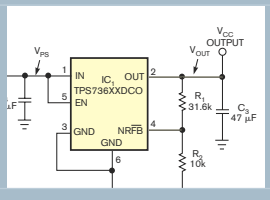

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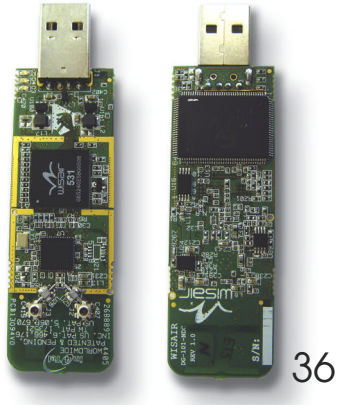

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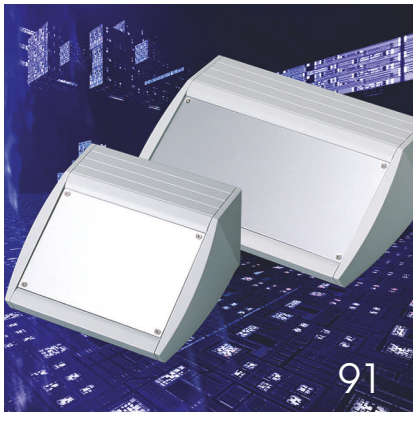

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DEPARTMENTS & COLUMNS

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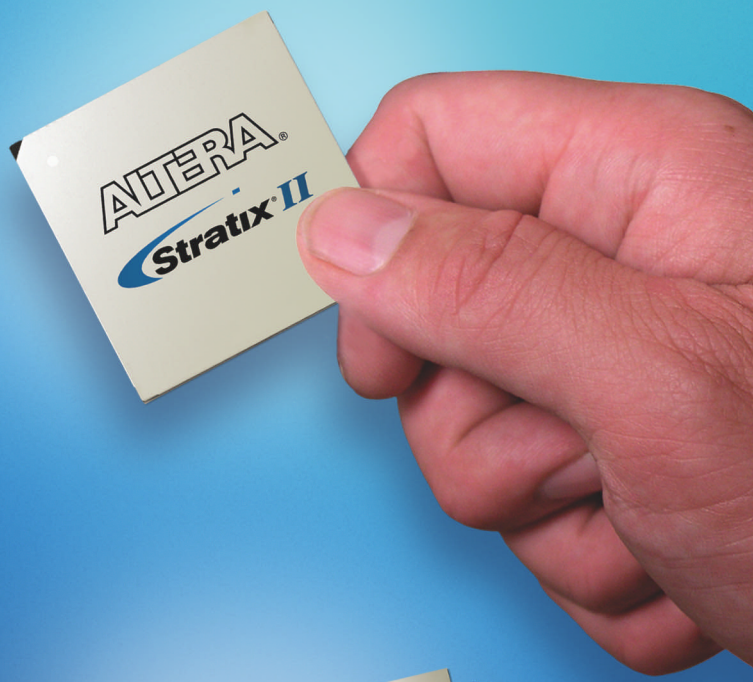

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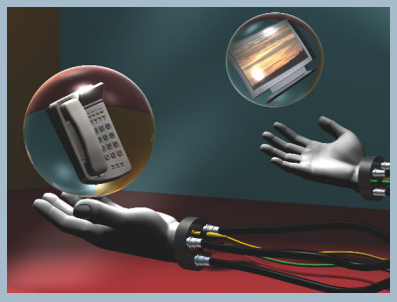

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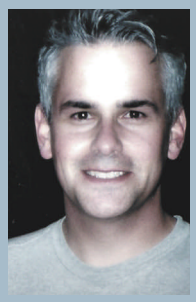

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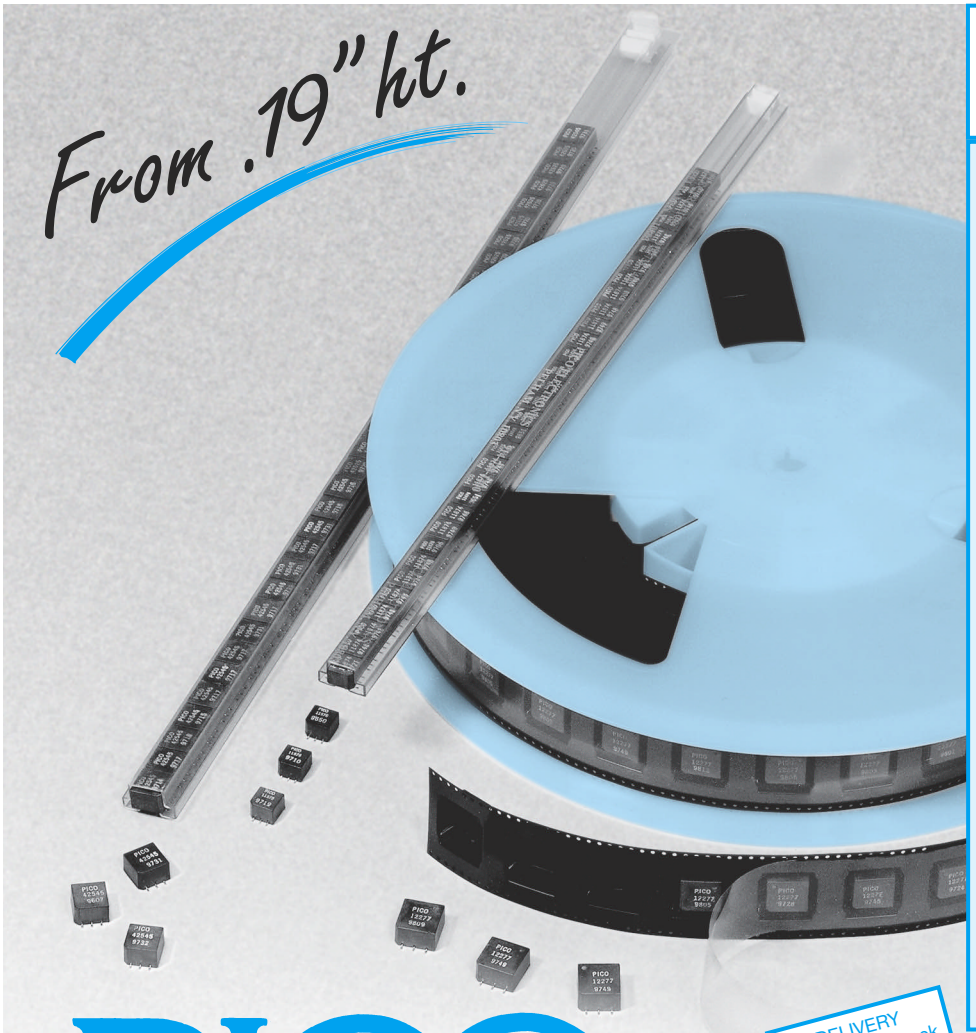

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BY MAURY WRIGHT, EDITOR IN CHIEF

HD-DVD and Blu-Ray lack wow at debut

I've followed the HD-DVD-versus-Blu-Ray skirmish for supremacy in next-generation DVDs for years. I think Sony (www.sony.com) cares little about the best technology or what's best for consumers and only about generating a royalty stream by having its IP (intellectual property) adopted as it did with audio CDs. Clearly, HD-DVD is a cheaper approach; old manufacturing equipment can make the HD-DVDs. And, despite what Sony may argue, Blu-Ray doesn't offer a superior picture, although it does offer a bit more storage capacity. Today, however, I'm of the opinion that consumers won't rush to either flavor—at least not to watch movies.

For several weeks, my family has been using a Toshiba (www.toshiba.com) HD-A1 HD-DVD player. (Watch for an account on the player's design in an upcoming *EDN* "Prying Eyes" story.)

The Toshiba player clearly offers a better picture than that of a standard DVD player. But the HD-DVD player doesn't provide the wow factor that DVD first offered over VHS tapes. And the HD-DVD experience isn't even in the same wow zip code compared with the first time I watched a live football game or even a TV drama in HD. In fact, a progressive-scan DVD player playing standard DVDs is almost as good as an HD-DVD player playing HD movies.

I haven't yet used a Blu-Ray player at home. And I know it's not always fair to compare the viewing experience in a store. But I was even more disappointed by Blu-Ray in a local store. I discussed the issue with our multimedia expert, Brian Dipert, and he speculates that Blu-Ray is inferior because available titles use older MPEG-2 encoding, whereas HD-DVD titles use MPEG-4. Ironically, Sony has continually pointed to the need to use MPEG-2 as a reason for the industry to adopt the higher capacity Blu-Ray technology.

Still, neither is going to win the hearts of consumers who want to watch movies. The list of available titles is sparse, and the popular ones cost around $30. I know both can play DVDs. But I can't see consumers moving in any significant numbers to a new player until the players are cheap. And I'm not suggesting the typical scenario in which mainstream buyers come after early adopters. I'm suggesting an even slower uptake.

Does that mean that HD-DVD and Blu-Ray drives won't sell before player prices hit $100? Not exactly. Certainly, computer applications such as back-up and archive will adopt the new storage technologies.

The game-console battle, however, will likely select the winner between HD-DVD and Blu-Ray. Today, Xbox 360 titles offer only 720-pixel resolution despite the fact that the console supports higher resolutions. Current DVD technology doesn't offer enough capacity to support higher resolutions and the lengthy story lines and capacious scenery in popular games. Both HD-DVD and Blu-Ray can enable more compelling games.

So, the real battle in the next-generation DVD market won't come down to movies or the $150 million promotional package that Microsoft (www.microsoft.com), HP (www.hp.com), Warner Brothers (www.warnerbros.com), Paramount (www.paramount.com), and others are planning to hype HD-DVD movies. Instead, it will likely come down to how Sony delivers on the PS3.

Just before I wrote this column, a number of blogs picked up a story about yields for the Cell processor being a huge problem for IBM (www.ibm.com)—which is making the chip for Sony. The story originated from an interview that our sister publication, *Electronic News*, did with an IBM executive (see www.reed-electronics.com/electronicnews/article/CA6350202). The executive may have been speaking only theoretically about yields for complex digital chips, but Sony did take a number of risks on the PS3, with both the choice of the Cell processor and the dependence on Blu-Ray.

Time will tell whether Sony can deliver PS3 this year in acceptable quantities and at the price target. Even if the company does, it will take a huge up-front loss from Cell yield problems and the expensive Blu-Ray choice. In the end, though, it may be game content that matters. But will the Cell processor really help Sony there? Today, in the Xbox 360, extra cores sit idle while software developers figure out how to harness available horsepower. Developers will have a tougher time taming the Cell. EDN

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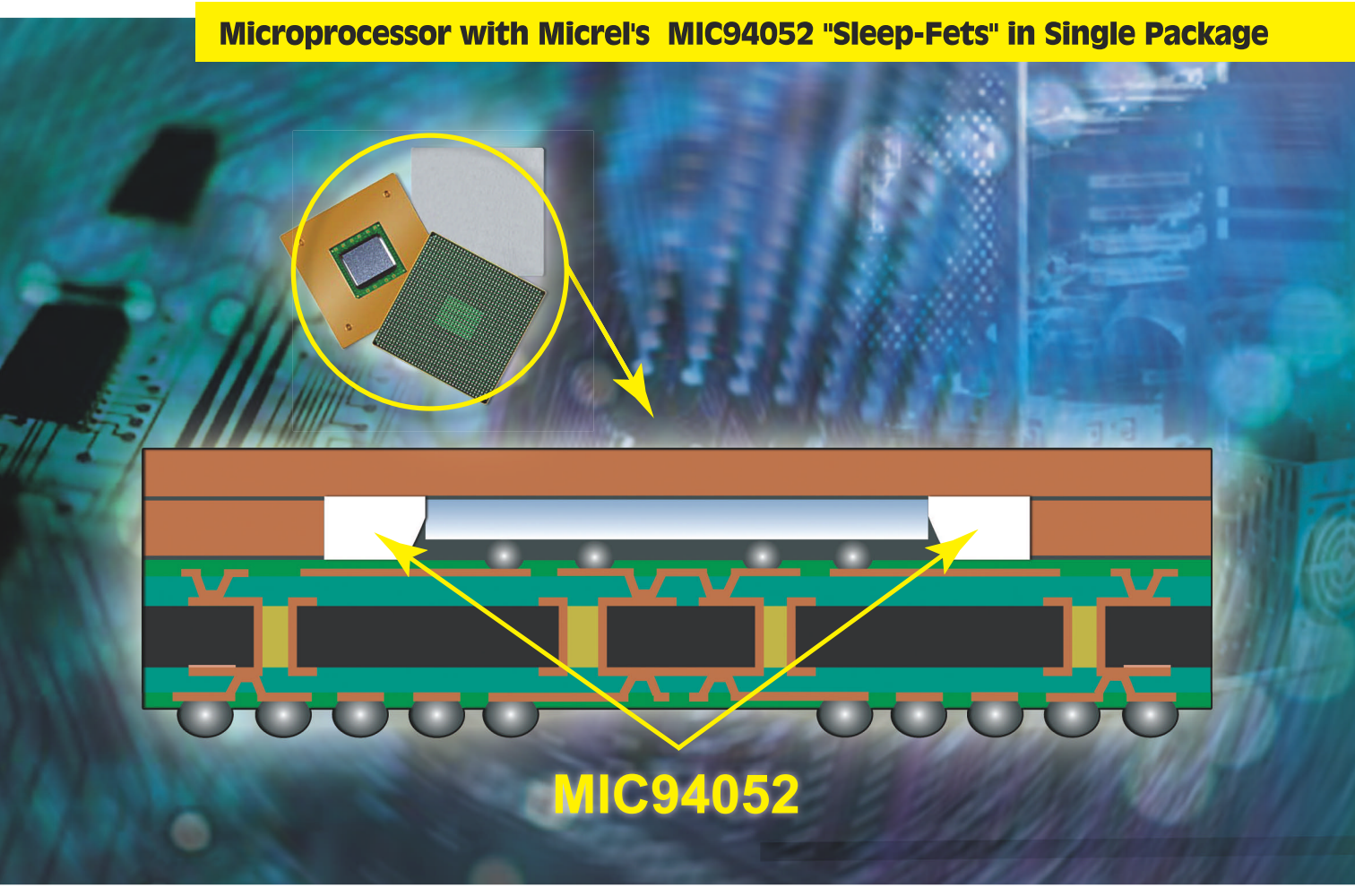

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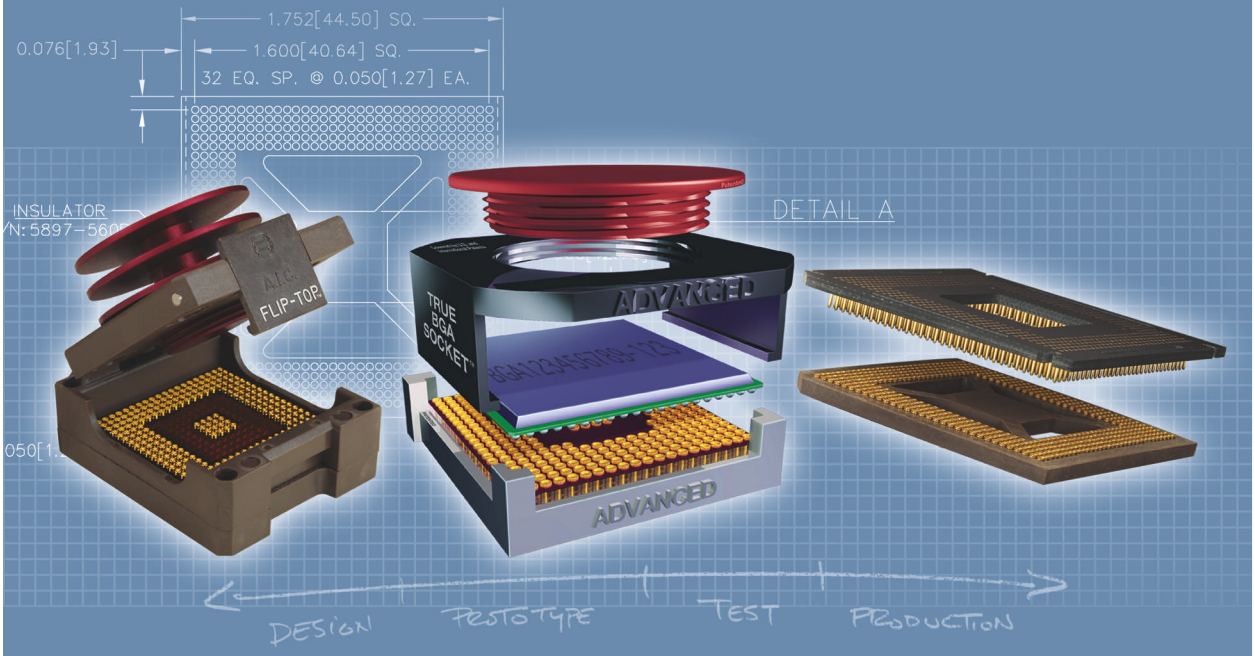

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No. 113

Optimizing Efficiency in White LED Backlight Applications

— By Dario Nurzad, Applications Engineer

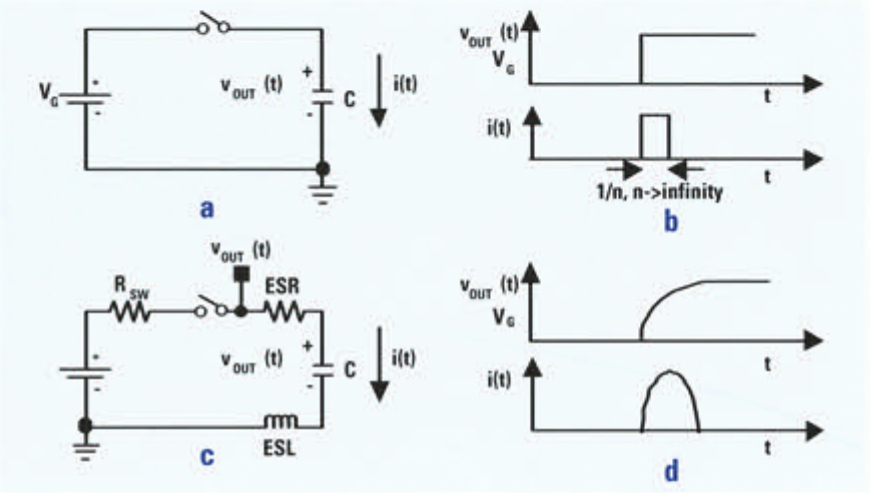

Figure 1. Charging a Capacitor From a Voltage Source (Both the ideal [a, b] and real [c, d] cases are shown)

White LEDs are typically driven with a constant DC current source to maintain constant luminosity. In portable applications with a single-cell Li-Ion source, the sum of the voltage drop across the white LED and the current source can be lower or higher than the battery voltage. This means that a white LED requires the battery voltage to be occasionally boosted. The best way to accomplish this is to use a step-up DC-DC converter. This method significantly optimizes efficiency at the expense of cost and PCB area. An alternative method of boosting the battery voltage is to use a charge pump, also called a switched capacitor converter. Here we will analyze in more detail the principle of operation of such a device.

Basic Principles of Charge Pumps

A capacitor is a component that stores electrical charge or energy for release at some predetermined rate and time. If an ideal capacitor is charged with an ideal voltage source V_G *(Figure 1a)* the charge storage occurs instantly

NEXT ISSUE:

Switching Controller Layouts

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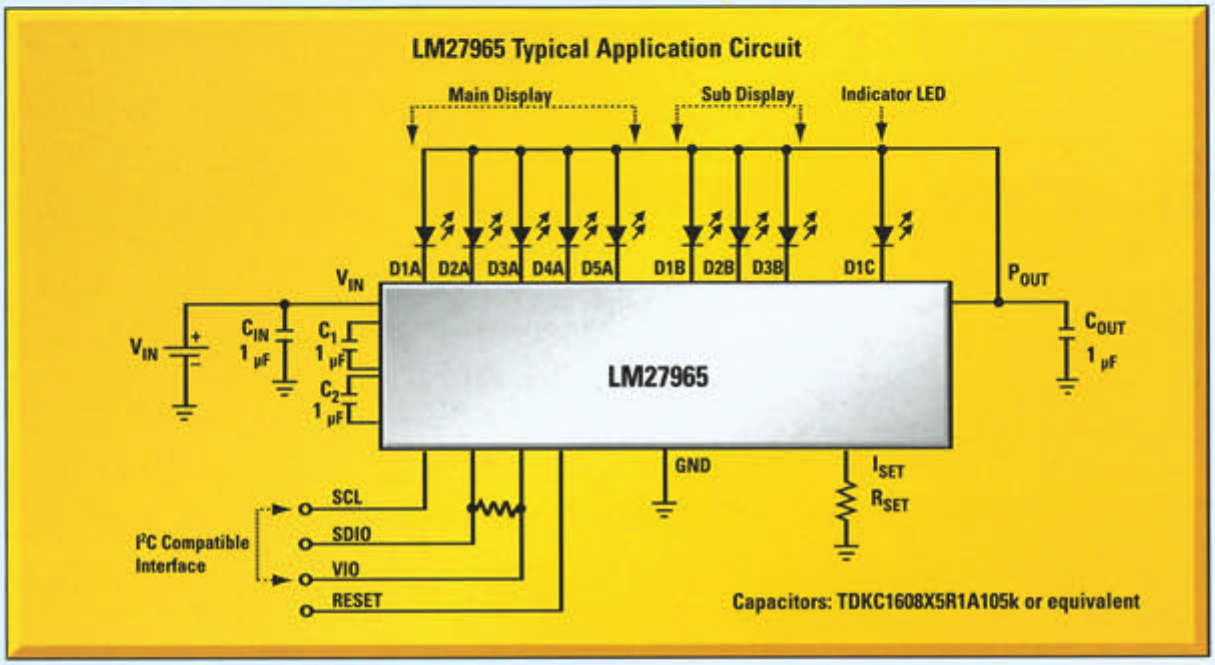
White LED Driver System with I²C Compatible Brightness Control

Inductorless LM27965 Drives Up to 9 LEDs at 91% Efficiency



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Optimizing Efficiency in White LED Backlight Applications

corresponding to a Dirac impulse function for the current *(Figure 1b)*. The total stored charge is given by: $Q = CV_G$.

Real capacitors have Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL). Neither affects the ability of the capacitor to store energy; however, they have a large effect on the overall efficiency of the switched capacitor voltage converter. An equivalent circuit for the charge of an actual capacitor is shown in *Figure 1c*, where R_{SW} is the resistance of the switch. The charging current path will have a series inductance, which can be reduced with proper component layout.

As soon as the circuit is energized, transient conditions of an exponential nature occur until a steady-state condition is reached. The capacitor parasitics limit the peak charge current and increase the charge transfer time *(Figure 1d)*. Therefore, the capacitor charge build-up cannot occur instantly, meaning that the initial voltage variation across the capacitor is equal to zero. Charge pumps use this property of capacitors as shown in *Figure 2a*.

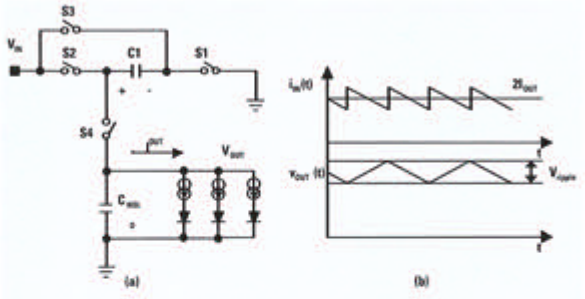

Figure 2. Charge Pump Circuit (a) with Relevant Waveforms (b)

The voltage conversion is achieved in two phases. During the first phase, switches S_1 and S_2 are closed, whereas switches S_3 and S_4 are open and are charged to the input voltage:

$$V_{C1+} - V_{C1-} = V_{C1+} = V_{IN}$$

During the second phase, switches S_3 and S_4 are closed, whereas switches S_1 and S_2 are open. Because the voltage drop across the capacitor cannot change instantly, the output voltage jumps to twice the value of the input voltage:

$$V_{C1+} - V_{C1-} = V_{OUT} - V_{IN} = V_{IN} \rightarrow V_{OUT} = 2V_{IN}$$

Voltage doubling can be accomplished using this technique. The duty cycle of the switching signal is usually 50%; which generally yields the optimal charge transfer efficiency. Let us examine in more detail the charge transfer procedure and how the switched capacitor converter parasitics influence its operation.

The steady-state current and voltage waveforms for a switched capacitor voltage doubler are shown in *Figure 2b*. Due to power conservation, the average input current is twice the output current. During the first phase, a charging current flows into C_1. The initial value of this charging current depends upon the initial voltage across C_1, the ESR of C_1, and the resistance of the switches. The charging current then decays exponentially as C_1 is charged. The charging time constant is several times greater than the switching period. Smaller time constants will cause the peak currents to increase. During this time the output capacitor C_{HOLD} supplies the load current discharging linearly by an amount equal to:

$$\Delta V_{OUT} = \frac{I_{OUT}}{2fC_{HOLD}}$$

During the second phase when C_1+ is connected to the output, a discharge current (whose magnitude is the same as the previous charging current,) flows through C_1 to the load. In this phase, the step change in the output capacitor current is approximately $2I_{OUT}$. Although this current step should create an output voltage step equal to $2I_{OUT}ESR_{C\_HOLD}$, the use of low-ESR ceramic capacitors renders this step change negligible. At this point, C_{HOLD} charges

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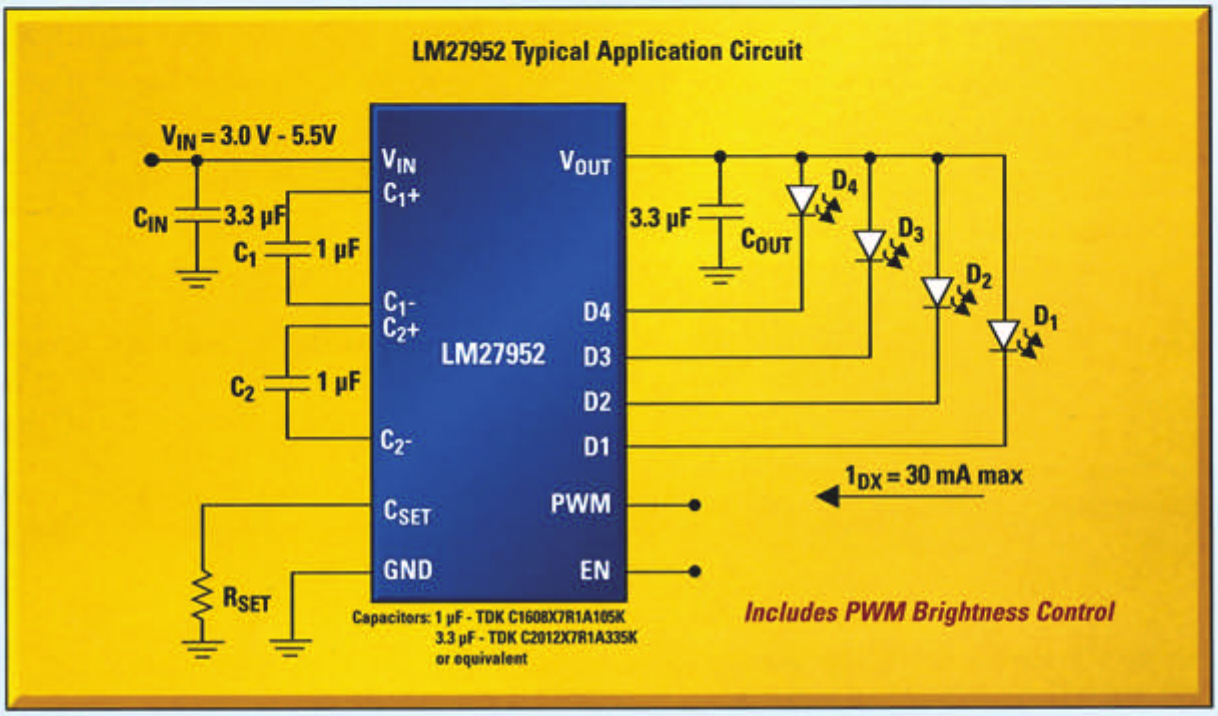

LM27952 Features

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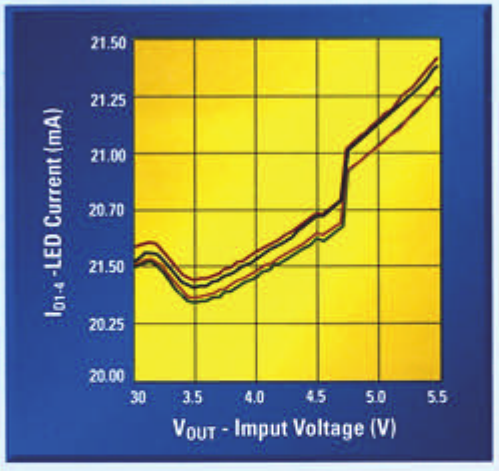

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linearly by an amount equal to: $\Delta V_{OUT} = \frac{I_{OUT}}{2fC_{HOLD}}$

When C_1 is connected back between the input and ground, C_{HOLD} discharges linearly by an amount equal to: $\Delta V_{OUT} = \frac{I_{OUT}}{2fC_{HOLD}}$

The total peak-to-peak output ripple voltage is given by: $V_{RIPPLE} \cong \frac{I_{OUT}}{2fC_{HOLD}}$

Higher switching frequencies allow smaller output capacitors for the same amount of ripple.

Parasitics of the charge pump cause the output voltage to fall as the load current increases. As a matter of fact, there is always an RMS current of $2I_{OUT}$ flowing through C_1 and two switches ($2R_{SW}$) resulting in a power dissipation of:

$$P_{SW} = (2I_{OUT})^2 (2R_{SW} + ESR_{C1}) = I^2_{OUT} (8R_{SW} + 4ESR_{C1})$$

In addition to these purely resistive losses, an RMS current of I_{OUT} flows through the equivalent resistance of the switching capacitor C_1:

$$P_{C1} = I^2_{OUT} R_{C1} = I^2_{OUT} \frac{1}{fC_1}$$

The RMS current flowing through C_{HOLD} is equal to I_{OUT}, resulting in a power dissipation of:

$$P_{ESR\_HOLD} = I^2_{OUT} ESR_{C\_HOLD}$$

All of the losses can be grouped in an equivalent output resistance:

$$R_{OUT} = 8R_{SW} + 4ESR_{C1} + \frac{1}{fC_1} + ESR_{C\_HOLD}$$

Thus the output voltage of the charge pump can be modeled as follows: $V_{OUT} = 2V_{IN} - I_{OUT}R_{OUT}$

In general, because of the low ESR of ceramic capacitors and the high switching frequency, the output ripple and output voltage drop depends on the switch resistances. Utilizing more switches and capacitors enables additional voltage conversions.

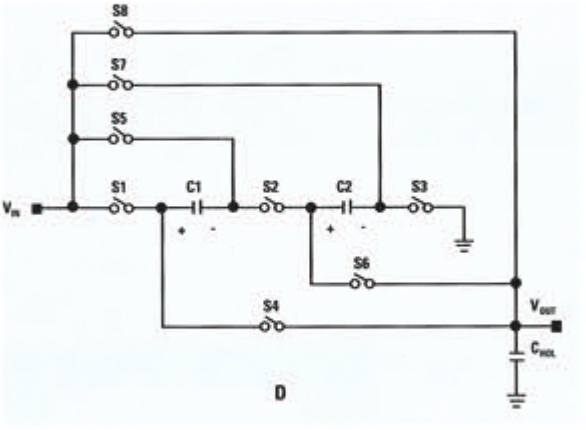

Figure 3. Switched Capacitor Circuit with 1x and 1.5x Gains

Figure 3 demonstrates this property using capacitors.

Once more, the voltage conversion is achieved in two phases. During the first phase switches S1 to S3 are closed, whereas switches S4 to S8 are open. Therefore C_1 and C_2 are stacked and—assuming C_1 equal to C_2— charged to half the input voltage:

$$V_{C1+} - V_{C1-} = V_{C2+} - V_{C2-} = \frac{V_{IN}}{2}$$

The output load current is provided by the output capacitor C_{HOLD}. As this capacitor discharges and the output voltage falls below the desired output voltage, the second phase is activated to boost the output voltage above this value. During the second phase, C_1 and C_2 are in parallel, tied between V_{IN} and V_{OUT}. Switches S4 to S7 are closed, whereas switches S1 to S3 and S8 are open. Because the voltage drop across the capacitor can not change instantly, the output voltage jumps to 1.5X the value of the input voltage:

$$V_{C1+} - V_{C1-} = V_{C2+} - V_{C2-} = V_{OUT} - V_{IN} = \frac{V_{IN}}{2} \Rightarrow V_{OUT} = \frac{3}{2} V_{IN}$$

The voltage boost operation is accomplished this way: A voltage conversion with a gain of 1x is achieved by closing switch S8 and leaving switches S1 to S7 open.

Dual-Display White LED Driver with 3/2x Switched Capacitor Boost

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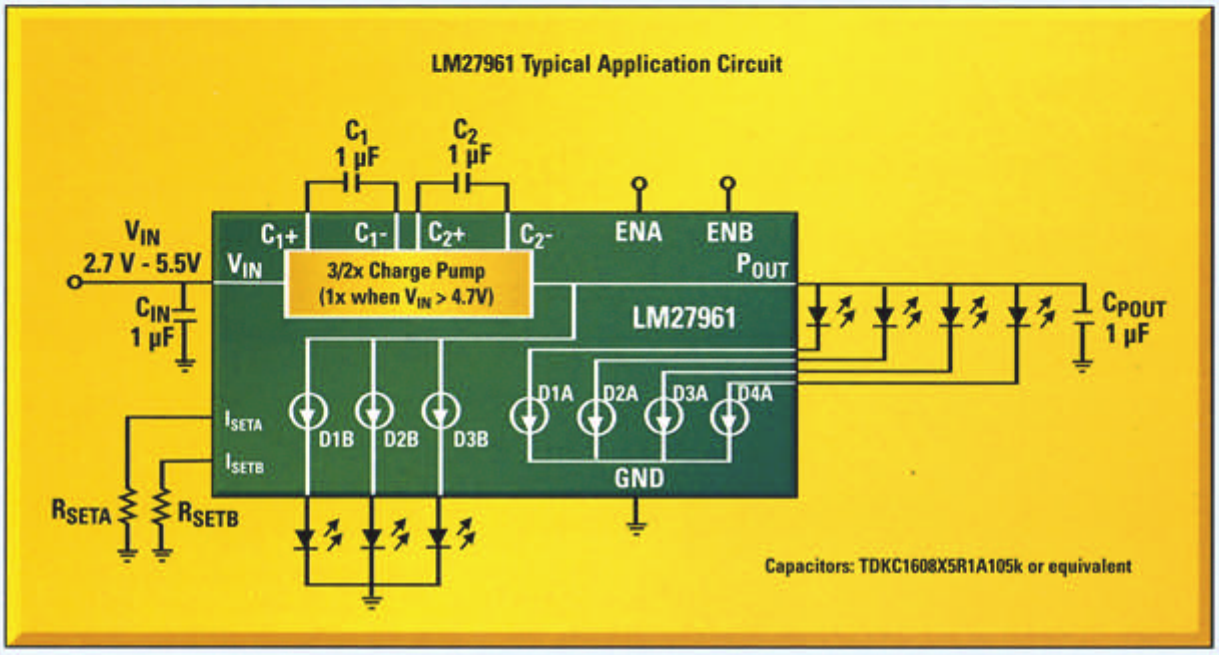

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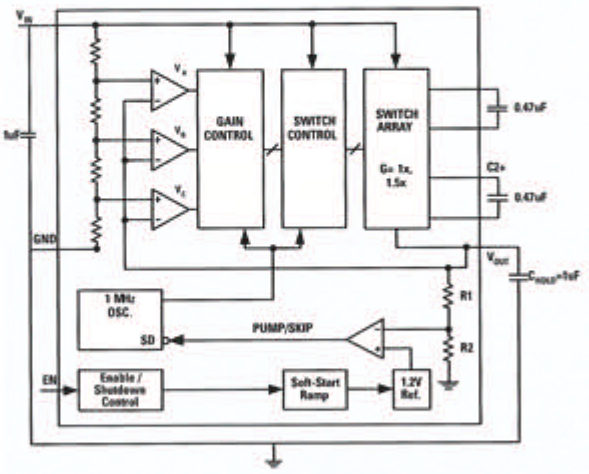

Figure 4. Switched Capacitor Regulator Block Diagram

Pulse Frequency Modulation (PFM) Scheme

A simplified Pulse Frequency Modulated (PFM) regulation scheme, which utilizes multiple gains, is depicted in *Figure 4*. The down-scaled output voltage is compared by the PUMP/SKIP comparator to a 1.2V voltage reference. The PUMP/SKIP comparator is ramped up linearly on start up to provide the soft-start function. When the output voltage is above the desired limit the device does not switch, consuming minimal supply current. During this idle state the output load current is provided by the output capacitor. As this capacitor discharges and the output voltage falls below the desired output voltage, the charge pump is activated until the output voltage is above this value again.

The primary advantage of the PFM regulation architecture is evident at light loads. Typically the load is provided with energy by the output capacitor. The supply current is very low, as the output capacitor only needs to be re-charged occasionally by enabling the charge pump.

In general, regulated charge pumps do not maintain a high efficiency over a wide input range. Because the input-to-output current ratio is scaled according to the basic voltage conversion, any output voltage magnitude less than the input-voltage-times-the-charge-pump-gain will result in additional power dissipation within the converter and efficiency will be degraded proportionally:

$$\eta_{IDEAL} = \frac{V_{OUT}\ I_{OUT}}{V_{IN}\ I_{IN}} = \frac{V_{OUT}\ I_{OUT}}{V_{IN}\ GI_{OUT}} = \frac{V_{OUT}}{V_{IN}\ G}$$

$$\eta_{IDEAL} \rightarrow 1 \Leftrightarrow V_{OUT} = GV_{IN}$$

The ability of the converter to change gains according to the input/output ratio allows for optimal efficiency over the entire input voltage range. Ideally, the gain should vary linearly. In reality, given a certain number of capacitors and switches, only a finite number of gain configurations are possible.

Referring to *Figure 4* the input voltage is scaled and fed into the non-inverting nodes of three comparators. All inverting nodes of the comparators are connected to the output voltage. Based on the input-to-output voltage ratio the outputs of the comparators provide the gain control circuitry with a three-bit word, which is used to select the minimum gain G, able to achieve the desired voltage conversion. In white LED applications, however, the selection of the proper gain G is not only based on the input and output voltages.

Conclusion

There are certain advantages in using switched capacitor rather than inductor-based switching techniques. An obvious advantage of switched capacitor converters is the elimination of the inductor and the related magnetic design issues. They usually have relatively low noise and minimal radiated EMI. Additionally, the applications circuits are simple and only a few small capacitors are needed.

Because there is no inductor, the final PCB component height is generally smaller than a comparable switching converter. ■

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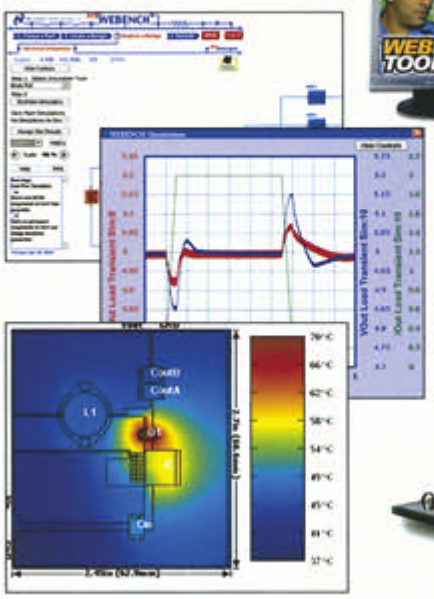

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USB counter/timer boasts 15 16-bit counters

Targeting a variety of measurement applications, including event counting, frequency measurements, position measurement, pulse counting, pulse-width modulation, and pulse generation, Acces I/O Products recently announced the USB-CTR-15 embedded digital counter/timer board. The board's plug-and-play features allow users to easily add counter/timer capabilities to any PC or embedded system with a USB 1.1 or USB 2.0 port. The USB-CTR-15 has a maximum input frequency of 10 MHz and includes five undedicated 82C54 counter/timer chips, each with three independent software-programmable, 16-bit counters. I/O-wiring connections are through a 50-pin IDC (insulation-displacement connector) or a removable screw-terminal-adapter board.

The board measures 3.550×3.775 in. and includes mounting holes compatible with the PC/104 form factor. The USB-CTR-15 supports use in most operating systems and includes a free Linux- and Windows-compatible software package with sample programs and source code in Visual Basic and C++. The USB-CTR-15 standard model with a steel enclosure is available now and sells for $249, and the board-only OEM version costs $199.

—by Warren Webb

▷**Acces I/O Products**, www.accesio.com.

The USB-CTR-15 embedded digital counter/timer board allows users to quickly add 15 software-programmable, 16-bit counters to any available USB port.

Quad-core DSP packs performance and features

The MSC8144 from Freescale packs four StarCore SC3400 DSP cores along with 10.5 Mbytes of internal memory, dual gigabit-Ethernet interfaces that support SGMII (serial-gigabit media-independent interface) and RGMII (reduced-gigabit media-independent interface), and a 16-bit UTOPIA (universal test and operations physical interface for ATM). The package also includes a 4×/1× Serial RapidIO interface and 2048 TDM (time-division-multiplexing) DS-0 channels to connect to PSTNs (public-switched-telephone networks). The MSC8144 targets wire-line- and wireless-infrastructure applications for voice, video, and data services. Additional on-chip peripherals include a DDR-I/II controller and a 66-MHz, 32-bit PCI-bus interface.

Freescale based the MSC8144 on the StarCore SC3400 DSP core. It includes a number of techniques to support a 1-GHz clock operating frequency. The SC3400 DSP core includes new SIMD (single-instruction-multiple-data) instructions, as well as exception and branch prediction. The SC3400 core includes instructions for Viterbi and video algorithms. Each core has a 16-kbyte instruction cache, a 32-kbyte data cache, and a memory-management unit. The device employs a quality-of-service technique for self-balancing the load. It employs user-transparent L2-cache-port interleaving to improve performance by 5 to 20%. The DMA auto initialization, granularity, and core-offload buffer-chaining scheme reduce the overhead of programming the core and improve memory efficiency, especially with SDRAM. Improvements in the pipeline limiter reduce the performance bottleneck for the TDM bus. The hardware-based background-cache-sweep operation helps avoid core stalls.

Because the SC3400 instruction set is a superset of the SC140 instructions, the MSC8144 software is fully binary- and assembly-code-compatible with Freescale's multiple- and single-core DSPs based on the StarCore technology. Freescale's CodeWarrior integrated development environment supports development for the MSC8144. It includes optimizing C/C++ compilers, profiling tools, cycle- and instruction-accurate simulators, device drivers, and operating systems. It comes with a hardware-development-platform and reference-board design. Enea's (www.enea.com) OSEck RTOS supports the MSC8144, with a pre-emptive and compact real-time kernel. The MSC8144 will be available for general sampling beginning in the third quarter of 2006 in 1-GHz and 800-MHz versions in a 783-pin, 29×29-mm FC-PBGA package for $180 (10,000).

—by Robert Cravotta

▷**Freescale**, www.freescale.com.

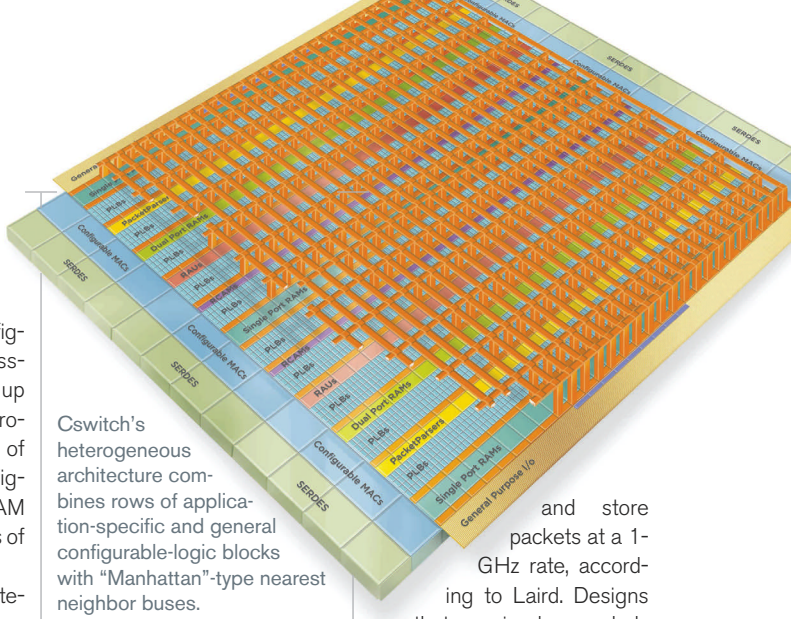
Radical FPGA takes on packet processing

Start-up Cswitch Corp this month introduced a novel configurable-logic chip targeting packet-processing applications in networking, wireless base stations, and telecom-infrastructure applications. The device comprises a heterogeneous array that interspersses rows of general-purpose logic cells—much like those in conventional FPGAs—with rows of SRAM-configured RAM and CAM (content-addressable-memory) blocks, ALUs (arithmetic-logic units), and specialized packet-processing blocks. The intent, according to the company's president and chief executive officer, Doug Laird, is to serve the growing number of applications that must process packetized data at wire speed with a device much faster and lower in power—for these applications—than a conventional FPGA but with much lower investment and time to market than an ASIC would require. In effect, the product is an application-specific FPGA.

I/O surrounds the configurable fabric. Configurable SERDES (serializer/deserializer) blocks, each of which can support PCI Express, XAUI (10-Gbit-attachment-unit-interface), Fibre Channel, or gigabit-Ethernet connections, line the chip. Similarly configurable MAC (media-access-controller) blocks back up these SERDES blocks. Programmable I/O pins, some of which can serve as configurable, high-speed DRAM ports, fill the other two edges of the die.

The fabric covering the interior of the die includes alternating rows of six kinds of configurable blocks. The most familiar of these, configurable-logic blocks, use a conventional four-input-look-up-table architecture. Rows of 1-GHz octal ALUs perform computational or statistical operations on packet contents. Packet-processing blocks parse headers and extract payloads at 800 MHz.

In support of these blocks, the chip provides rows of 1-GHz specialized memory blocks that you can configure as RAM, primary CAM, or tertiary CAMs for buffering, address mapping, pattern searching, or even, with clever use of the other blocks, general-expression processing. The chip also has rows of conventional single- and dual-port RAMs. The application-specific architecture provides smaller blocks of dual-port RAM, assuming that they will act as interblock-buffer memories, and larger blocks of single-port RAM for parameter and packet storage.



Cswitch's heterogeneous architecture combines rows of application-specific and general configurable-logic blocks with "Manhattan"-type nearest neighbor buses.

Interconnect for the chip differs dramatically from that for general-purpose FPGAs. Because designers can express most data-plane-packet processing as data-flow architectures, Cswitch eliminates the use of the elaborate mesh of varying-length, varying-orientation interconnect segments typical of an FPGA in favor of simple, nearest neighbor, orthogonal routing. These short segments are fast and 20 bits wide, and you can subdivide them into groups of 5 bits. Each terminates in a registered, fully populated crossbar switch that connects the interconnect segments into the logic fabric and to each other. Thus, a flow-through datapath design that uses nearest neighbor interconnection becomes a fully registered pipeline. This approach allows the chip to receive, edit, classify, and store packets at a 1-GHz rate, according to Laird. Designs that require less orderly interconnect must daisy-chain signals through segments and crossbars, resulting in longer—but highly predictable—interconnect delays.

The utility of such a design depends on its tools, for which Cswitch has partnered with Magma Design Automation (www.magma-da.com), establishing a design flow that incorporates Blast Create and Blast FPGA tools, along with application-specific libraries and Cswitch-specific mapping and timing files. Designs for implementation in the Cswitch chip would typically combine complex library functions, explicit instances of the various Cswitch configurable blocks, and Verilog. Magma is inferring Cswitch structures directly from Verilog, according to Magma product director, Sanjay Bali, but only for relatively obvious cases, such as mapping combinatorial logic onto the logic blocks and multiplications onto the ALUs.

So far, Cswitch has done test chips of the SERDES blocks with its foundry, Chartered Semiconductor (www.charteredsemi.com), in its 90-nm CMOS process. Laird expects a full tape-out of the company's high-end chip in September.

–by Ron Wilson

▷**Cswitch Corp**, www.cswitch.com.

DILBERT *By Scott Adams*

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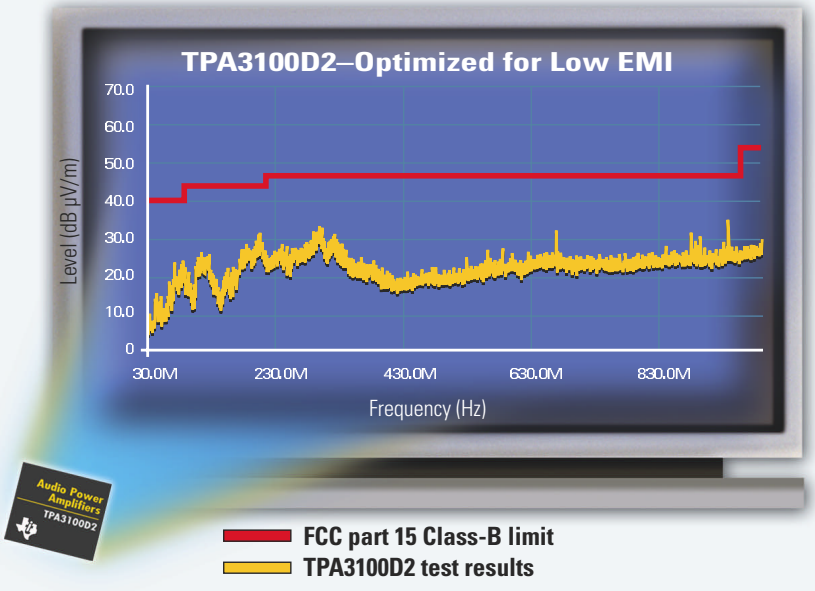

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Digital-power controllers offer digital and analog architecture

Since *EDN* last covered digital-power controllers, three more digital-power-controller ICs have appeared: Microchip's new part is a close-the-loop-digitally device; Maxim's is a hybrid approach in that the control loop is still analog, but the power management and communication are digital; and Primarion's new addition to its Di-POL (point-of-load) family uses a PID-control loop (see "Digital power lures system architects, power-supply vendors," *EDN*, May 25, 2006, pg 46, www.edn.com/article/CA6335298). When you add this influx of parts to the digital-control and -management parts from Texas Instruments (www.ti.com), Zilker Labs (www.zilkerlabs.com), and Silicon Labs (www.silabs.com), you get the indication that power-supply-chip vendors view digital power as worth their serious attention (see "A bit-o'-power: digitally controlled power conversion," *EDN*, July 21, 2005, pg 59, www.edn.com/article/CA624951).

Microchip's dsPIC30F1010/202X family relies on the company's DSC (digital-signal-control) engine to deliver a complete digital-power-control loop with 1-nsec PWM (pulse-width-modulation) resolution and 2M-sample/sec performance from its built-in 10-bit ADC.

Unlike digital-power controllers that rely on a dedicated hardware-PID controller, the chips do not adhere to any one control algorithm or topology. "Any algorithm you can conceive, you can code up," says Brian Kris, staff architect for Microchip. In addition, direct communication between the ADC, the PWM, and the analog comparators in the form of a configurable control fabric allows you to configure their intercommunication upon start-up. For example, says Kris, "You can automate the precise taking of voltage and current measurements during each cycle and trigger an asynchronous conversion process." The parts also have multiple analog comparators that allow you to select from a variety of input references to modify the behavior of the PWM generators—for example, to assert the output of the PWM generator for feedforward compensation. Prices for the two-chip set start at $2.99.

Like the previous member of Primarion's Di-POL family of digital-power controllers, the PX7510, the PX7520 is PID-control-loop-based. The new part offers dual-phase-control capability at a switching frequency of 150 kHz to 2 MHz in addition to the Di-POL-family features, such as a PMBus/I²C serial interface, a library of 60 common PMBus commands, internal voltage and temperature referencing, and an internal oscillator. Linear Technology (www.linear.com) will act as a second source for the part.

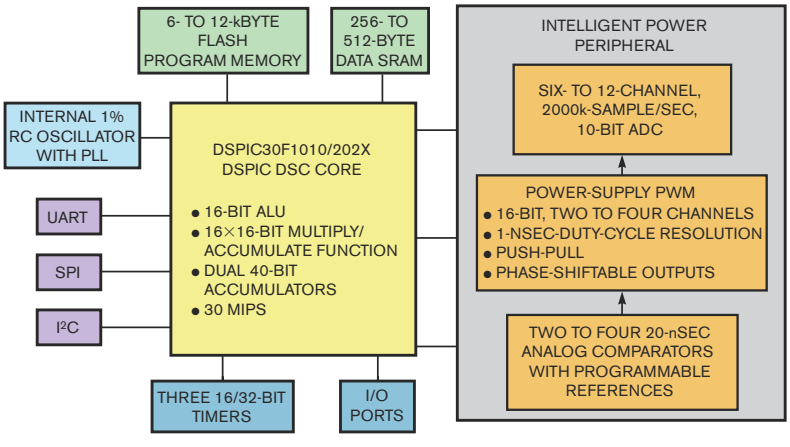
The MAX8688 from Maxim serves designers seeking to add digital-power-communication and -management ability to legacy analog power supplies. The chip interfaces with the system controller through the PMBus, sending and receiving system-level control queries and commands, such as peak-temperature, output-current, and output-voltage data for all of the power-subsystem modules. This approach allows the system controller to poll each module at fixed intervals and log the information for future analysis of field failures. The chip taps into the enable node, the feedback node, or the reference input of the power supply's analog-control circuitry to provide voltage tracking and sequencing, as well as setting the output voltage at within ±0.2% accuracy over the −40 to +85°C industrial-temperature range. The MAX8688 requires a 3.3V±10% supply voltage and can control output voltages of 0 to 5.5V. Prices start at $1.95.

—by Margery Conner

▷**Microchip**, www.microchip.com.

▷**Primarion**, www.primarion.com.

▷**Maxim**, www.maxim-ic.com.



Microchip's programmable DSC engine allows you to implement any control algorithm in the dsPIC 30F1010/202X digital-power controller, and the control fabric linking the DSC, the PWM, the analog comparators, and the 10-bit ADC allows the topology to change based on transient conditions.

FROM THE VAULT

"It may not be true right now, but the time will come when the cost of MSI (medium-scale integration) will become lower than the cost of the boards that it goes on. And today, the interconnection cost for MSI is still significant when compared to the cost to duplicate the same job with LSI (large-scale integration)."

Bob Noyce, then president of Intel, *EDN*, Sept 15, 1971

2.4 GHz and Sub-1 GHz RF ICs

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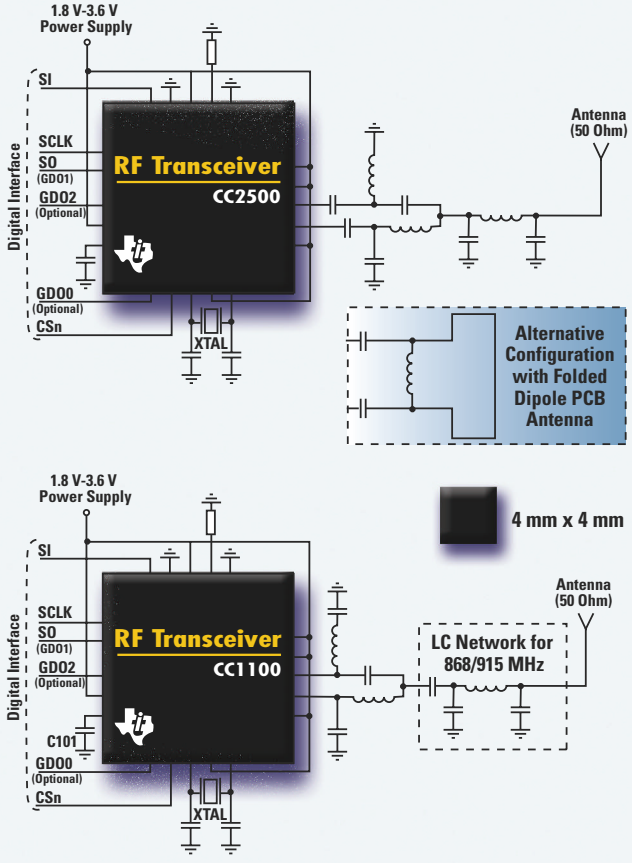

The new **CC2500** and **CC1100** RF transceivers from Texas Instruments are the industry's lowest system cost, multi-channel radios for low-power wireless applications. Operating in the 2.4 GHz (CC2500) and sub-1 GHz (CC1100) frequency bands, the devices include several useful digital features like full packet handling, FIFO buffers, clear channel assessment, wake-on-radio and more.

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VOICES

Digi's Joel Young

Building better networks

Joel Young is both vice president of research and development and chief technical officer at Digi International, where he leads projects to simplify device networking. He has a bachelor's degree in electrical engineering and a master's in computer science from the University of Southern California (Los Angeles). He is on the board of directors for the ITA (Industrial Telecommunications Association) and is vice president for the Nebraska Center for Excellence in Electronics.

Why did you pick engineering as a profession?

A I've always been a problem solver, a dreamer, and a tinkerer. When I was growing up, after coming to the conclusion that I wasn't going to be one of the childhood favorites, like police officer, firefighter, professional athlete, or garbage collector, I discovered that there was the profession called engineering for which people actually got paid to solve hard problems, dream, and tinker. I think this idea was cemented in high school when I got to start doing the really cool math.

Can you briefly summarize the engineering background that led to your current position?

A I started with Bell Laboratories designing signaling protocols for the voice network. I became part of a team implementing Signaling System No. 7. This step started me on the path to deploying new database systems in the AT&T network and eventually down the management path. I took the experience to directing R&D at a small start-up-like company, which made encryption modules and radios. After five years, I found myself at Digi International, where I have been for the past five years. Digi was not then into telecom, wireless, security, or embedded modules. Today, we are into all of those things, so previous experience has really helped.

"We've tried outsourcing a fair amount of work in the past, but I find that the outsourced engineering isn't good enough at creative problem solving."

What are the biggest technical challenges that you face in your segment of the industry?

A I don't know whether you would directly call them technical, but they are certainly implementation challenges. The biggest two are figuring out ways to get quality, customized products to market faster and faster and deciding on the combination or right mix of wired and wireless technologies for a market or application. It doesn't always work to ask your customers, because sometimes they don't know [what they want] until they have it.

What type of engineering talent do you look for, and is it difficult to find?

A First, we look for creative problem solvers and good communicators. That's not to say that we don't look for pure engineering skills, but people can learn engineering skills. We've tried outsourcing a fair amount of work in the past, but I find that the outsourced engineering isn't good enough at creative problem solving.

How will the trend toward engineering outsourcing affect future projects?

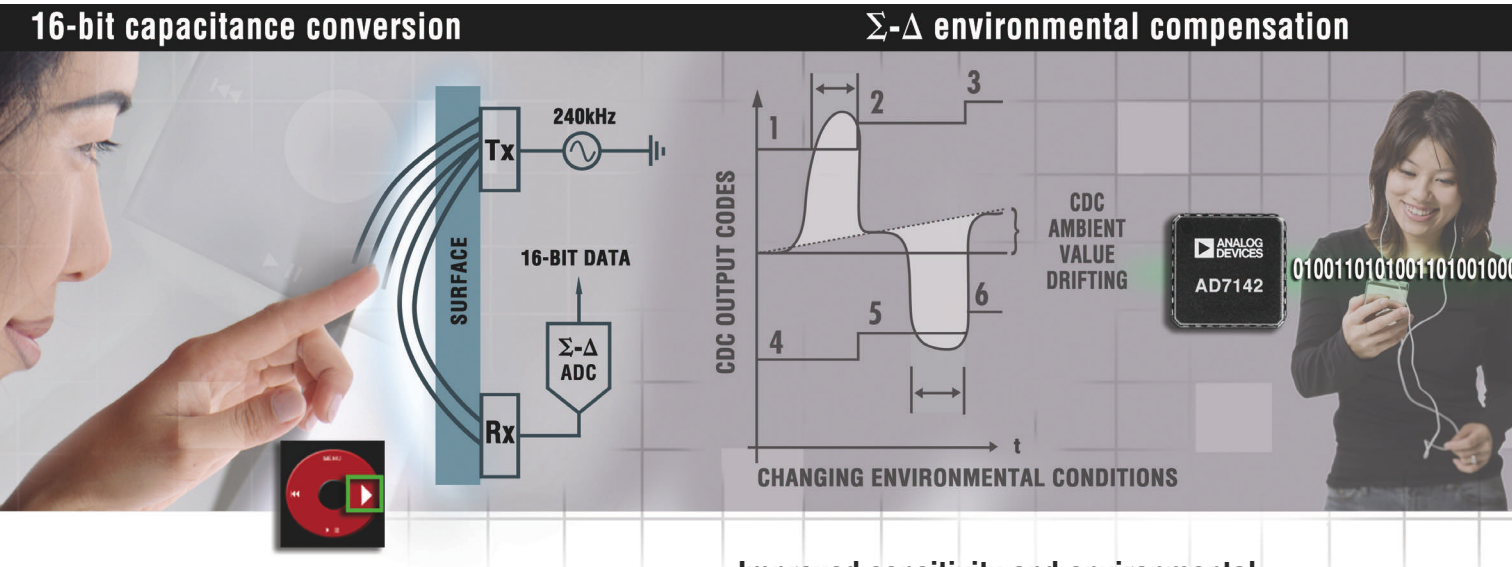
A I don't plan on doing outsourcing for anything that requires a creative solution or intellectual-property development. I've found it works better internally. We might still return to outsourcing some of our low-creativity maintenance-of-line work, but I don't have any immediate plans for this step. I must add, however, that our company has changed a lot over the past few years. When I started, we had more than 100 engineers in pretty much one location in the United States. Now, we have a few more in engineering, but they are scattered over more than 10 locations, including Europe. As such, we have had to become skilled at remote engineering management.

What do you do for fun?

A In true engineering form, there are many dimensions to this answer. I love to build things; it doesn't matter whether with wood or wires. However, for unwinding, nothing beats sitting down and cranking on my Les Paul or Strat guitars. Fortunately, my children now like to play them, as well. As a family activity, camping is at the top of the list.

–by Warren Webb

16-bit touch controller for the best user experience.
In data conversion, analog is everywhere.



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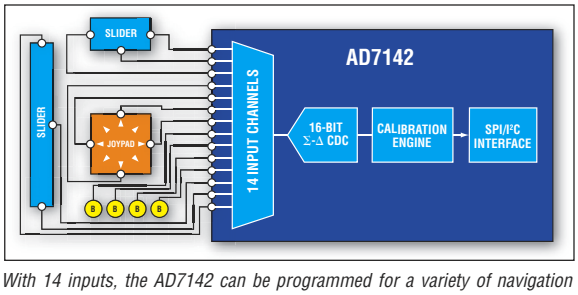

With 14 inputs, the AD7142 can be programmed for a variety of navigation functions including buttons, sliders, scroll wheels, and joypads.

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ANALOG DEVICES

GLOBAL DESIGNER

ETSI adds IP support to DAB, simplifying a DVB-H migration

Despite the efforts by Nokia (www.nokia.com) and Qualcomm to guide the deployment of mobile-TV services to DVB-H (digital-video-broadcasting-handheld) and MediaFlo technologies, respectively, those aren't the only choices. Giant British Telecom, for instance, stated early this year that it would roll out digital-radio and -TV services to handsets using DAB (digital-audio-broadcasting) technology. The company plans to offer its DAB-based Movio this summer with service provider Virgin Mobile (www.virginmobileusa.com). Detractors, however, believe DAB is far inferior to DVB-H in video quality and the number of channels that it offers. So, many are welcoming the fact that standards body ETSI (European Telecommunications Standards Institute) has just revised the DAB standard to include support for the delivery of multimedia streams over IP (Internet Protocol), much like the technique that the DVB-H standard, which ETSI also controls, specifies.

Realistically, British Telecom had little choice in selecting DAB. The frequencies that DVB-H uses are unavailable in the United Kingdom and won't for several years be free of analog-TV use. Now, however, British Telecom will have the flexibility of migrating its IP-based service to multiple network technologies, including DVB-H and even Wi-Fi.

—by Maury Wright

▷**British Telecom**, www.bt.com.
▷**ETSI**, www.etsi.org.
▷**Qualcomm**, www.qualcomm.com.

CHINESE FAB GETS POPULAR IP BLOCKS

Chinese fab SMIC (Semiconductor Manufacturing International Corp) has just added plans to support IP (intellectual-property) cores from ARM in 90-nm-chip designs. The two companies announced that SMIC would offer ARM's low-power Metro cores and high-performance Advantage cores. The Metro family targets portable devices with power concerns, and the Advantage cores fit a variety of performance-centric networking, communications, and computing applications. The cores will be available to SMIC customers by the fourth quarter of 2006.

—by Maury Wright

▷**SMIC**, www.smics.com.
▷**ARM**, www.arm.com.

Main players will pick DVB-H for mobile TV

The mobile-TV technology that finally dominates will employ open standards and a competitive market, according to Nokia. "The analogy here is GSM [global system for mobile communication], which made possible personal telephony and affordable terminals," says Harri Mannisto, director of multimedia business at Nokia. "This was based on open standards and a competitive ecosystem, and you have the same possibility here for DVB-H [digital-video broadcast-handheld], which will succeed for personal TV and video."

Mannisto dismisses the idea of devices with multiple mobile-TV technologies, in contrast to Qualcomm, which has announced that it is working on a chip that will support its own MediaFlo technology, along with DVB-H and ISDB-T (integrated services digital broadcasting-terrestrial). "In the '90s, there was a lot of talk about DECT [digital enhanced cordless telecommunication] and GSM, but you don't hear that now," says Mannisto. "The mainstream has gone with the scale, and I believe the same thing will happen here. There'll be a lot of trials of technologies and some experimentation, but the main players will go with scale, and we believe that's DVB-H."

Yoram Solomon, senior director of mobile connectivity at Texas Instruments, also believes that DVB-H will win out against others, including DMB-T (digital multimedia broadcasting for television), ISDB-T, and MediaFlo, but believes that the mobile-phone network will provide a complementary system. "DVB-H is going to be the primary live, streaming model, but, if you want to watch replays or video on demand, then you're going to go to cellular. Cellular is not going away," says Solomon.

—by Melanie Reynolds, Features Editor, *Electronics Weekly*

▶**Nokia**, www.nokia.com.
▶**Qualcomm**, www.qualcomm.com.
▶**Texas Instruments**, www.ti.com.

Some handhelds, such as the MM-7400, can play video content from MobiTV (www.mobitv.com) and other sources (courtesy Sanyo, www.sanyo.com).

06.08.03

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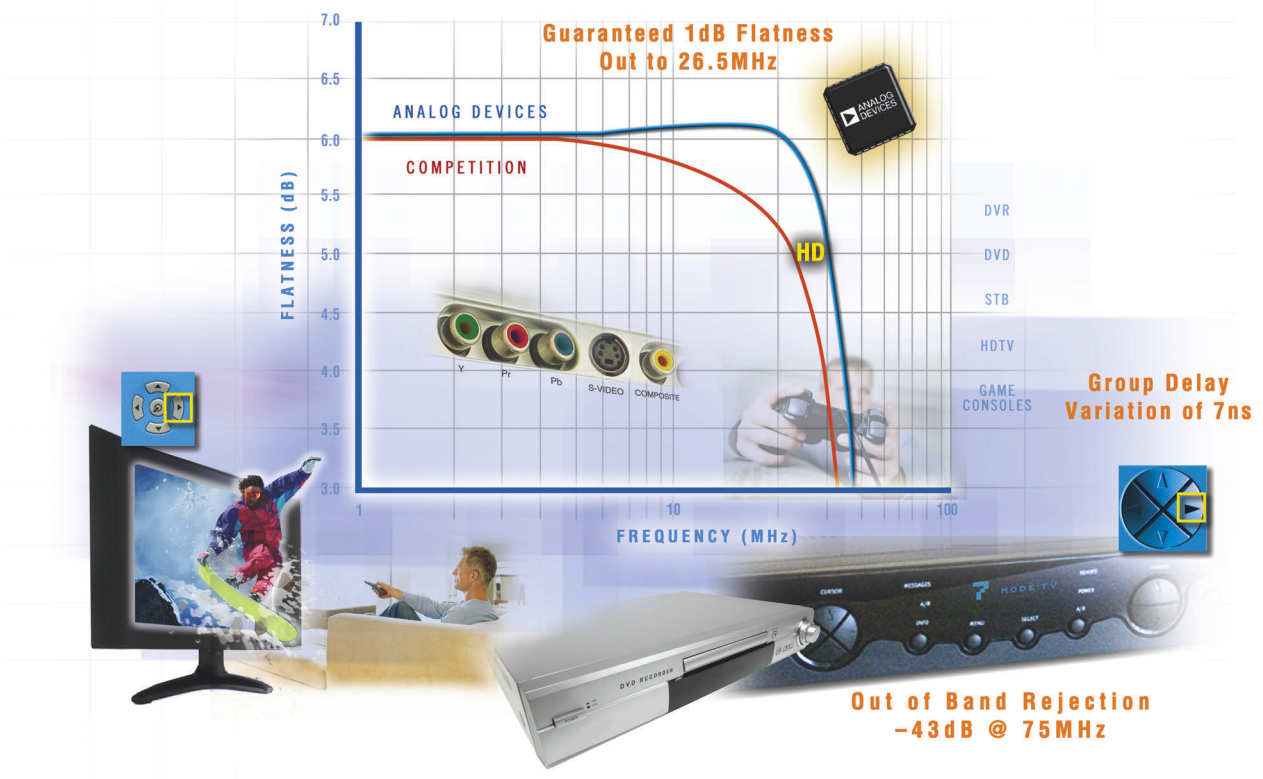

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ANALOG DEVICES

BY BONNIE BAKER

Sallen-Key lowpass-filter stopband limitations

When you design an analog, lowpass, antialiasing filter, you would expect its gain amplitude to continuously decrease beyond the filter's cutoff frequency. For the most part, this assumption is a safe one, but it's not necessarily true with the classic Sallen-Key lowpass-filter design. The Sallen-Key filter attenuates any signals in the frequency range above the cutoff frequency to a point, and then the response turns around and starts to increase in gain with frequency.

Figure 1 illustrates the behavior of three Sallen-Key lowpass filters using signal-supply amplifiers. In the top three curves, the diagram captures the open-loop gain of each amplifier as the response crosses 0 dB. During this test, the configuration for all three amplifiers is a dc noise gain of 1000V/V, or 60 dB. In the diagram, the bandwidth of op amps A, B, and C are 38 MHz, 2 MHz, and 300 kHz, respectively.

A second set of three curves in this **figure** shows the frequency response of second-order, Sallen-Key lowpass filters for each amplifier. The data indicates that the lowpass filters are performing as you would expect for a little more than a decade after the cutoff frequency of 1 kHz. Although the approximation method does not impact or correct this unexpected behavior, these filters use a Butterworth design. After the cutoff frequency, all three of the filter's responses show a slope of −40 dB/decade. You would expect this response from a second-order lowpass filter. Then, at some point, the filter gain begins to increase at a rate of 20 dB/decade. The difference in the frequency response at the point at which the three amplifiers change to a positive slope depends on the amplifier's output impedance. As the amplifier's open-loop gain decreases, its closed-loop output resistance increases. Eventually, each filter's response flattens at the 0-dB crossing frequency of the op amp's open-loop gain. It is no coincidence that the "flattening" of the filter response occurs at this crossing. As the frequency increases beyond this point, the amplifier's gain is less than 0 dB.

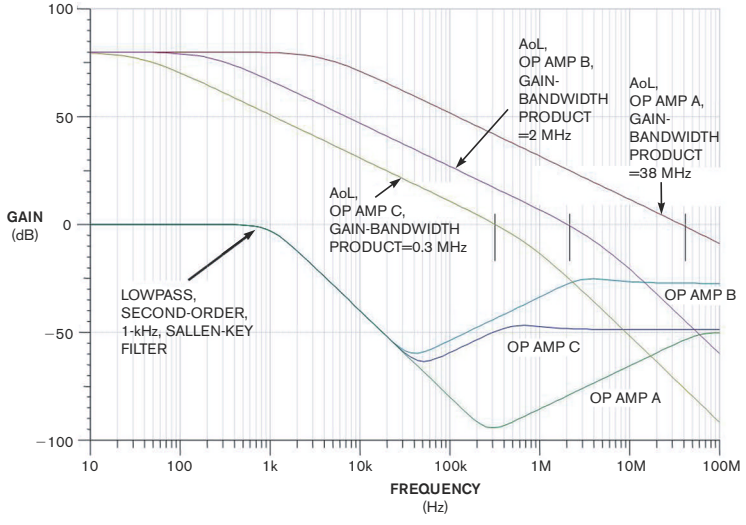

Figure 1 Note the frequency response of three Butterworth, second-order lowpass filters, along with the amplifier gain of each amplifier. The configuration for all three filters is Sallen-Key. The amplifier-gain curves start at the top of the diagram at 60 dB, and the filter curves start at 0 dB.

If you use a Sallen-Key lowpass filter, some characterization is in order. You can reduce the impact of the upward trend in the filter's response by following the offending active filter with a passive RC lowpass filter. The caveat to this action is that the following filter may interfere with the phase response of your intended filter, which may cause additional ringing in the time domain. Further, this action also creates a stage whose output is not low-impedance.

Alternative filters can solve the problem without adding an RC filter. When an inverting filter is an acceptable alternative, you can use a multiple-feedback circuit,which does not display this reversal in the gain response at higher frequencies and does not swing the input stage's common-mode voltage.EDN

Bonnie Baker is a senior applications engineer at Texas Instruments and author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie@ti.com.*

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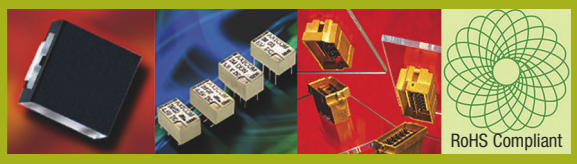

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Wireless USB in a dongle

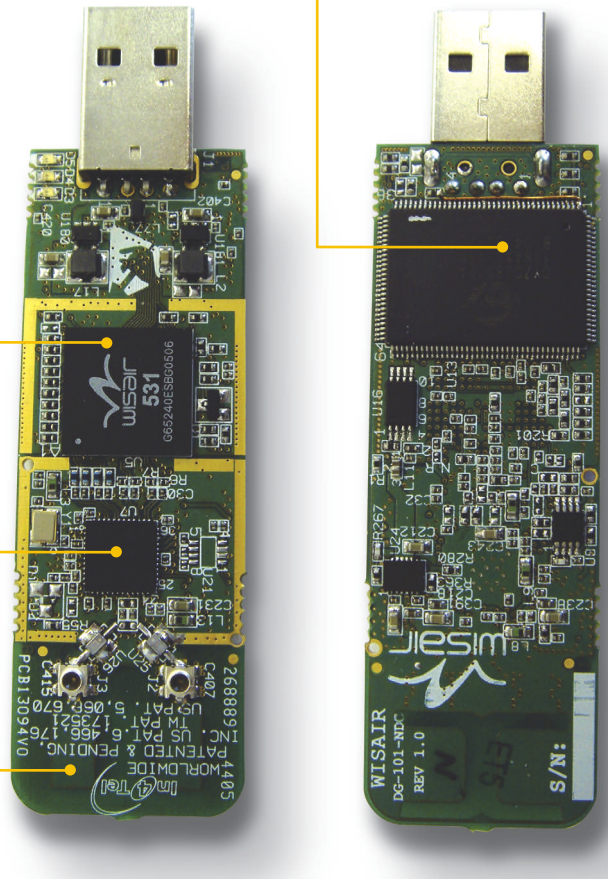
The promise of wireless USB seems unbeatable—eliminate all those little, somehow inflexible cables that make a rat's nest of everyone's desktops, and turn where to put the printer into a spatial-visualization test. But in reality, unless you have a large number of peripherals, wireless-USB equipment has to be extremely compact and inexpensive to avoid being more of a hassle than those stinking wires. Therefore, in turn, the dongle that turns a USB port on the PC into a wireless base station has to exploit the greatest possible level of integration. But a single chip combining a USB wired interface, controller, wireless baseband, and RF is still technically a little out of reach. Here's a look at how one vendor, Wisair, is approaching the problem today with a production-ready reference design.

A wireless-USB hub starts with a connection to the bus. Seeing no differential advantage in designing its own USB interface until it could integrate it into a single chip, Wisair purchased the wired-USB transceiver, protocol engine, RAM, and general-purpose microcontroller for its dongle in one package—in what appears to be a Cypress Semiconductor 7C68013A USB high-speed peripheral chip. Doing so gives it a fast 8051 and 16 kbytes of memory to work with for system control, interfacing the USB port to the wireless-baseband device and driving the activity-monitor LEDs.

The Cypress USB controller attaches directly to Wisair's 531 baseband/MAC (media-access-controller) chip. This device, which Wisair designed in 130-nm CMOS, creates everything but the RF portion of a WiMedia UWB (ultrawideband) radio platform. The chip permits the wireless-USB link to operate at 53 to 480 Mbps and still coexist with nearby Bluetooth and 802.11a/b/g transceivers without external filters.

The Wisair 531 teams with a 180-nm SiGe (silicon-germanium) BiCMOS RF device, the Wisair 502 wireless-USB PHY (physical layer). The 502 is a full OFDM (orthogonal-frequency-division-multiplexing) RF section, deploying three 528-MHz UWB subbands within the 3.1- to 4.8-GHz band. To aid integration, the chip requires less than 10 external components, including only one crystal, and a integrates both a voltage-controlled oscillator and a bandpass filter. The chip supports two-way antenna diversity, and the company claims that the device achieves effective bit rates to 480 Mbps at ranges of greater than 10m.

Taking advantage of the RF chip's ability to handle two antennas, the reference design provides two loop antennas embedded in the pc board. Note that they are both in the same plane, keeping everything compact but limiting the ability of antenna diversity to capture difficult signals. The silver connectors at the bases of the antennas are test points.



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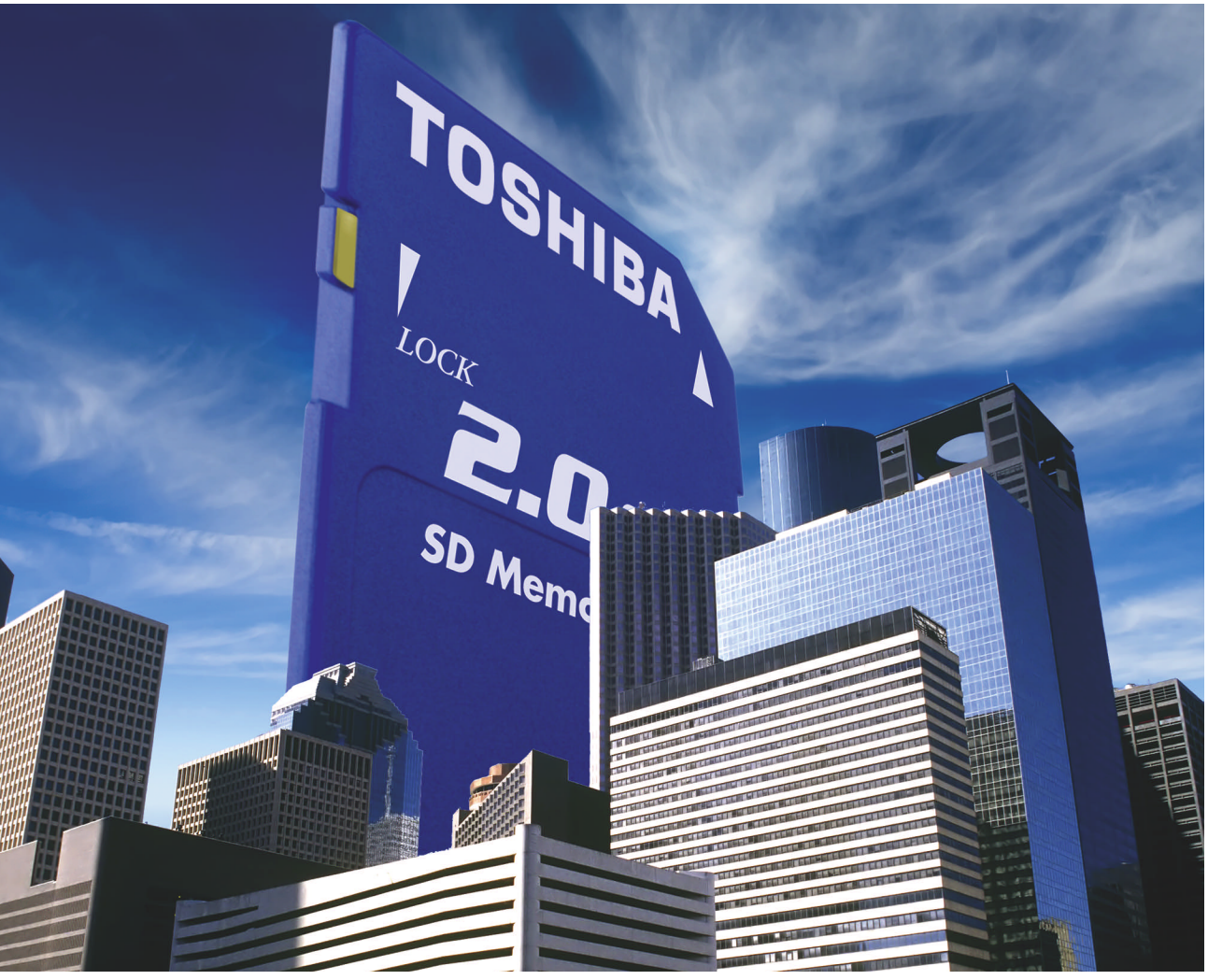

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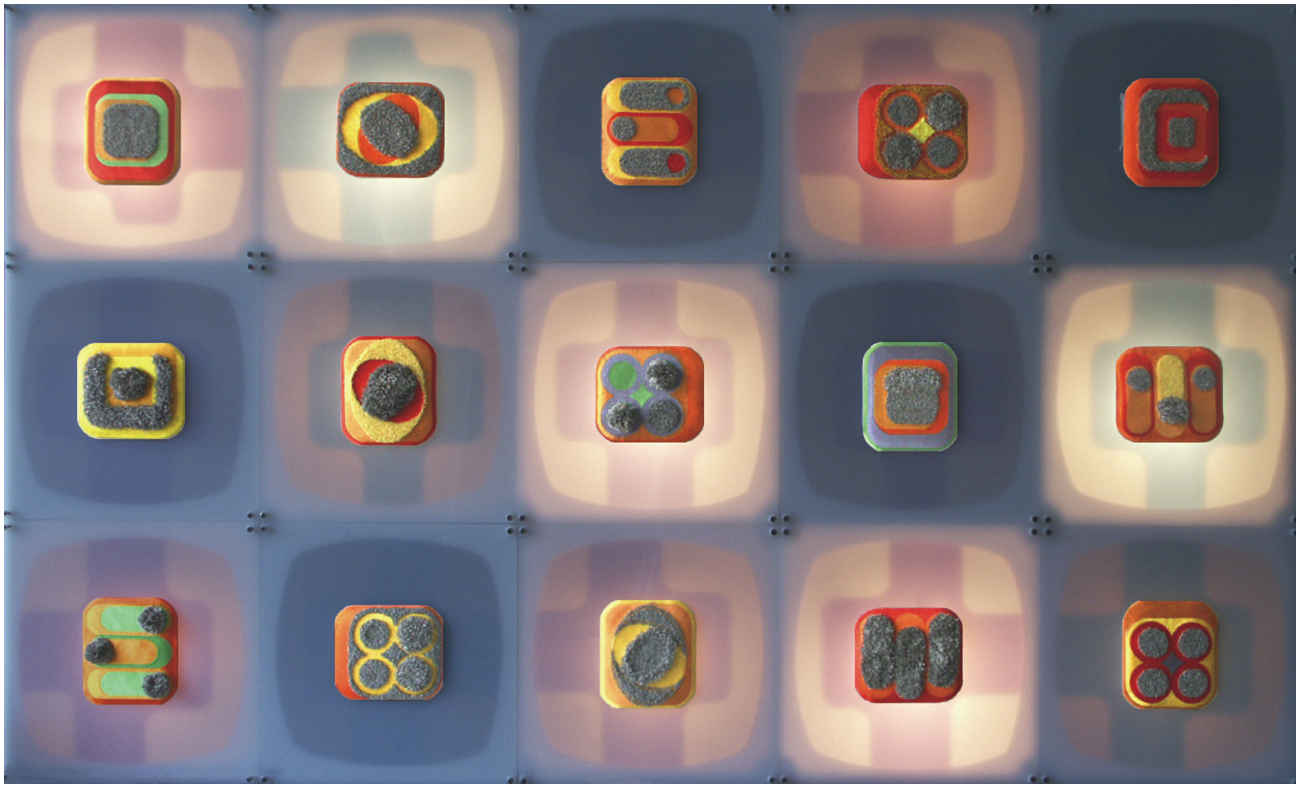

COURTESY INTERNATIONAL FASHION MACHINES

FABRICS GET SMART

ELECTROACTIVE TEXTILES SERVE AS SWITCHES, SENSORS, AND MORE.

BY JOSEPH OGANDO • SENIOR EDITOR, *DESIGN NEWS*

If your idea of smart fabrics is a pair of khaki pants that sheds food stains, think again. The smartest fabrics are becoming electroactive, allowing them to address far more important engineering problems than whether you wear your lunch to an afternoon meeting. These textiles can help you build flexible sensing systems, detect chemicals, generate mobile power, and perform other tasks. "More than 70% of the surfaces we interact with daily are textiles. Once those textiles can carry data and electrical power, it opens up a huge new world of applications," says Stacey Burr, president of Textronics Inc, a developer of smart-fabric technology.

Rather than just a single material, electroactive smart fabrics encompass many combinations of textiles and electrically conductive materials. Though manufacturers often base smart fabrics on elastomeric fibers, such as Lycra, they can also create them from a wide variety of synthetic and even natural fibers. Various knit, woven, and nonwoven fabrics can all be smart, too. As for the electrical properties, smart fabrics most commonly contain fine metal wires, either in the yarn of the fabric or in the fabric alongside ordinary textile fibers. Other smart fabrics get their electrical properties from ICPs (inherently conductive polymers) or nanocomposites deposited as coatings on the fabric's fibers.

All of these electroactive smart fabrics have a way to go before they become commonplace engineering materials. Some of the textiles, particularly those that rely on nanotechnology, are available only in quantities suitable for development work. Others, although fully commercial, may not have enough of a track record to alleviate the kinds of technical concerns that design engineers bring up within minutes of evaluating a technology. "Smart fabric is still something of a black art," says Maggie Orth, president and founder of International Fashion Machines, a developer of smart-fabric products.

Smart-fabric suppliers, for example, all make compelling arguments for the use of their technologies in various sensing systems. But only one company, NanoSonic Inc, provides technical data about sensor performance—in this case, strain range, linearity, and hysteresis.

This lack of basic engineering information may somewhat limit the use of smart fabrics. Spyros Photopoulos, an analyst who studies the smart-fabric market for Venture Development Corp (www.vdc.com), recently surveyed OEMs regarding their plans for using smart fabrics and

AT A GLANCE

- Smart fabrics encompass many combinations of textiles and electrically conductive materials.
- Physically integrating fabrics with traditional rigid electronics requires new approaches to interfaces and interconnections.
- Carefully look at and test the current-carrying capability of prospective textiles. Fibers may burn up when you subject them to harsh electrical environments.
- One of smart fabrics' biggest potentials is their ability to sense strain and serve in pressure-monitoring systems.

Figure 1 Users can roll, crumple, or fold Eleksen's textile pressure sensor, which finds use in keyboards for mobile electronics.

found that many expressed doubts about the durability and performance of smart fabrics. "Price is also a big issue," he says. "Many OEMs wouldn't consider smart-fabric technology without strong consumer demand."

Smart fabrics may also suffer from a division within the design community. "Electrical engineers and textile designers don't speak the same language," says Textronics' Burr. And bringing these two groups together goes beyond semantics. Engineers need to know how to physically integrate fabrics with traditional rigid electronics, which requires new approaches to interface and interconnect designs (see **sidebar** "Proceed with caution").

PROCEED WITH CAUTION

Few people know more about working with smart fabrics than Maggie Orth. She did her doctoral work on them at the Massachusetts Institute of Technology (Cambridge). She consults on smart fabrics for OEMs. She founded International Fashion Machines, which makes smart-fabric products, and she has created smart-fabric art. Another electronic-textile supplier even calls her the godmother of smart-fabric technology.

So it's probably worth listening to her when she says that design engineers need to move cautiously when considering whether they want to use electronic smart fabrics. "The thing about textiles is that there are lots of ways to do things," she says. "There are also a lot of ways to mess up." To avoid messing up, Orth asks some tough questions at the beginning of any application she works on. Here are three important ones:

How will you connect the textiles to the other electronics? **"I don't even start a project if I don't know how I'm going to connect all the electronics," she says, before noting that traditional connections sometimes won't work with "fussy" e-textiles. Take soldering, for instance. "Most textiles won't stand up to soldering temperatures." And rigid connectors can interfere with the design goals that pushed you into textiles in the first place. Over the years, she has had to come up with a number of nontraditional ways to marry electronic textiles with rigid electronics. She has even tied knots onto pc boards.**

Have you accounted for unfamiliar failure modes? **"Remember that the 'e' in 'e-texile' stands for 'electronic,' which means that you're putting electronics into products that didn't formerly have them," she says. E-textile products often need to be machine-washable, for example, or they need to be ironed. They may also go through extreme flex cycles that could break the continuity of the conductive material. Remember, too, that flexibility in textiles goes beyond understanding a minimum radius as you would for a flexible circuit. "Flexibility in textiles is different," Orth says, explaining that users can often fold, crumple, and twist textiles in ways that a flex circuit need not endure.**

How much juice can the textile really handle? **Orth advises engineers to carefully look at–and test–the current-carrying capability of prospective e-textiles. They currently have no standard electrical ratings, and the suppliers don't or can't reveal the gauge of the tiny wires in a given textile. "Some of these wires are no bigger than the fiber itself," Orth says, adding that, in some cases, yarns burned up when designers subjected them to electrical loads similar to what they'd see in use.**

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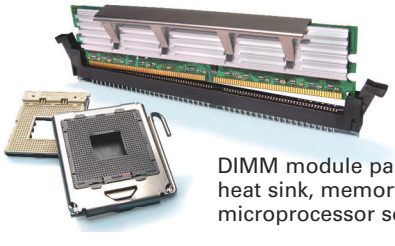

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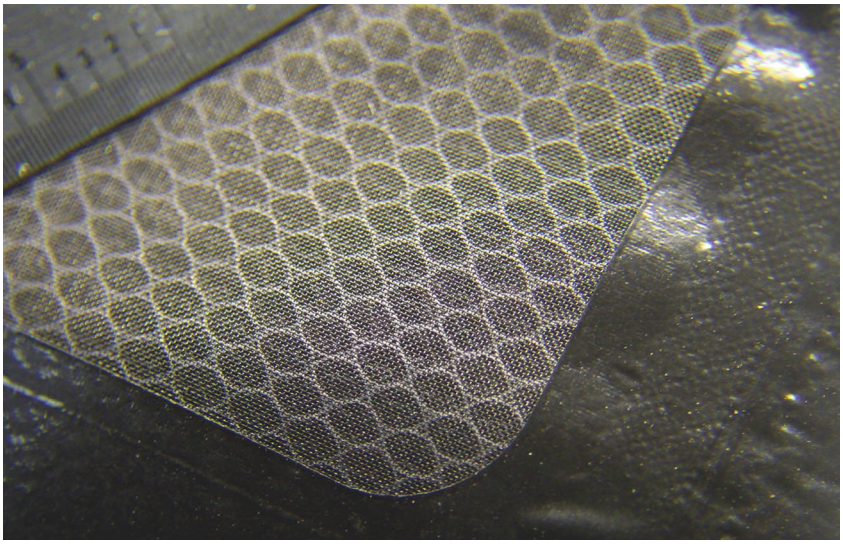

Figure 2 The ElekTex sensor contains a proprietary e-textile that senses pressure. It works by measuring voltage drop across the sensor surface.

The smart-fabric applications that have moved the furthest commercially have involved switches and controls for consumer electronics. The leader in this field, Eleksen Ltd, has supplied touch-sensitive fabric controls for products ranging from electronics cases to ski jackets with integrated, machine-washable controls for audio players. The company has also developed portable, wireless fabric keyboards that you can roll, fold, or even crumple (**Figure 1**).

Eleksen makes these fabric controls from a multilayered fabric containing three electroactive layers. Two outer conductive layers surround an inner resistive layer that separates the conductive layers until someone presses them together, says Andrew Newman, product manager at Eleksen and one of the technology's developers. Eleksen then measures the voltage drop at various points on the surfaces to determine where and how hard someone presses the fabric. "We measure the interaction in the x, y, and z directions," says Newman, who adds that the z-axis measurement gives a relative, rather than an absolute, pressure reading.

The company can supply a variety of configurations, including single switches or arrays of switches on a given fabric surface. The company's keyboards, for example, use the array-of-switches approach. Newman notes that Eleksen's fabric, ElekTex, and the related electronics, output an analog signal (**Figure 2**). So, you can apply the same technology to sliding control buttons, such as those for volume or scrolling on a computer display.

Although ElekTex applications currently focus squarely on consumer electronics, Newman sees some potential for a variety of human-to-machine interface applications. In automotive interiors and appliances, the technology could find use in software-configurable control panels that can cover even deeply curved surfaces. In one of the only indications of smart-fabric durability, Eleksen has performed extensive mechanical testing of its products, including subjecting them to 10 million press cycles and hysteresis tests after 30,000 roll-up and folding cycles. "That's far in excess of what they would see in real life," says Newman (**Reference 1**).

Figure 3 International Fashion Machines' reimagined household light switch costs $129 and is UL-approved.

Another switch application comes from International Fashion Machines. Orth has reimagined the ordinary household light switch as a capacitive touch sensor in the shape of a pom-pom (**Figure 3**). At first glance, pom-pom switches may seem frivolous. But consider that Orth gets $129 for her light switch, which has appeared in museum shows, compared with approximately $2 for the ugly, plastic commodity versions at the hardware store. "Smart fabrics allowed me to create a premium product," she says. She's also got UL approval—no easy task—for her switch.

SENSE STRAIN AND MORE

For engineers, one of the biggest technological potentials for smart fabrics relates to their ability to sense strain and serve as the basis for pressure-monitoring systems. Both broad types of smart fabric—those based on metal wires and those based on ICPs or nanocomposites—can perform some sensing. Whatever the type of fabric, they tend to operate on the fabric equivalent of the piezoresistive principle. With fabrics based on metal wires, such as those from Textronics, the movement of the fabric itself brings conductive metal fibers closer together or farther apart, altering the resistance of the fabric. Something similar happens with fibers incorporating ICPs or nanocomposites, in that strain changes the electron transport between conductive clusters on the fabric fiber. With some signal processing, these resistance changes translate into pressure measurements. "In theory, you can turn all kinds of resistive materials into strain sensors," says Orth.

Two of the newest ways to create fabric sensors rely on nanotechnology to make polymer-fabric fibers conductive to varying degrees. NanoSonic has recently developed smart fabrics it based on an electrostatic self-assembly process (**Reference 2**). The developers of this process initially created it to make free-standing elastomeric sensor films. The self-assembly process can infuse the surface of textile

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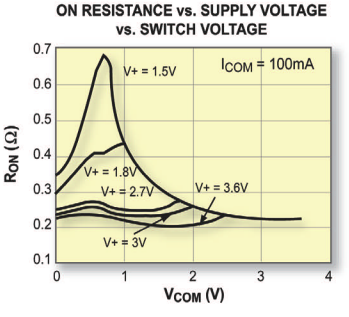
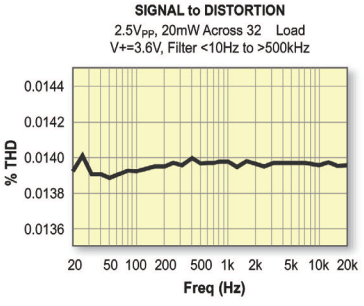
	ISL84715	SPST (NO)	0.26	0.04	4kV	1.6 to 3.6	SC70-5
	ISL84716	SPST (NC)	0.26	0.04	4kV	1.6 to 3.6	SC70-5
	ISL43L210	SPDT/2:1 Mux	0.44	0.06	6kV	1.1 to 4.5	SC70-6
	ISL43L110	SPST (NO)	0.26	0.04	4kV	1.1 to 4.5	SC70-5
	ISL43L111	SPST (NC)	0.26	0.04	4kV	1.1 to 4.5	SC70-5
Duals	ISL84762	2xSPDT/2:1 Mux	0.29	0.03	9kV	1.6 to 3.6	TDFN, MSOP
	ISL84684	2xSPDT/2:1 Mux	0.29	0.03	9kV	1.6 to 3.6	TDFN, MSOP
	ISL8484	2xSPDT/2:1 Mux	0.29	0.03	9kV	1.6 to 4.5	TDFN, MSOP
	ISL43L220	2xSPDT/2:1 Mux	0.23	0.03	9kV	1.1 to 4.5	TDFN
	ISL43L410	DPDT/Diff 2:1 Mux	0.29	0.03	9kV	1.1 to 4.5	TDFN, MSOP
	ISL43L120	SPST (NO)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L121	SPST (NC)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L122	SPST (Mix)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L710	Diff SPST (NO)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L711	Diff SPST (NC)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
	ISL43L712	Diff SPST (Mix)	0.17	0.008	8kV	1.6 to 3.6	TDFN, MSOP
Quads	ISL83699	Dual DPDT/Diff 2:1 Mux	0.3	0.06	9/4kV	1.6 to 3.6	QFN, TSSOP
	ISL84780	Dual DPDT/Diff 2:1 Mux	0.45	0.07	4kV	1.6 to 3.6	TQFN, TSSOP
	ISL8499	Dual DPDT/Diff 2:1 Mux	0.3	0.06	9/4kV	1.6 to 4.5	QFN, TSSOP
	ISL43L420	Dual DPDT/Diff 2:1 Mux	0.3	0.06	9/4kV	1.1 to 4.5	QFN
Octals	ISL84781	8:1 Mux	0.41	0.056	4kV	1.6 to 3.6	TQFN, TSSOP
	ISL84782	Diff 4:1 Mux	0.5	0.056	4kV	1.6 to 3.6	TQFN, TSSOP
	ISL43L840	Dual 4:1 Mux	0.5	0.056	4kV	1.6 to 3.6	QFN, TSSOP
	ISL43L841	Diff: 4:1 Mux	0.5	0.056	4kV	1.6 to 4.5	TQFN, TSSOP

ISL84684 Typical Performance





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fibers with various nanocomposites—combinations of polymers and metals or metal oxides. Fabrics incorporating these fibers have high conductivity, with bulk resistivity values of 10^{-5} Ω-cm, according to Andrea Hill, a NanoSonic researcher who helped develop the conductive fabrics.

They also can tolerate extreme elongations. Rick Claus, NanoSonic president and founder, notes that the original sensor films, metal rubber, can measure strains as high as 1000% with full-scale linearity of 1%. At lower strains, they can tolerate thousands of flex cycles and exhibit low mechanical hysteresis, he adds. The new fabric versions, metal-rubber textiles, can tolerate similarly large strains.

Another twist on inherently conducting fibers comes from Eeonyx. The company has a proprietary process for coating textiles with ICPs based on doped polypyrrole. The company polymerizes the materials on the surface of the fabric itself so that the coating material fills interstices in the surface and forms a physical bond with the fibers. Jamshid Avloni, the company's president, reports that the ICP's conductivity doesn't match the level that metal wires offer. But, then again, it doesn't have to.

"There are orders of magnitude of difference between the conductivity of, say, polyester and copper," says Avloni. "We occupy a middle ground." The company can deliver fabrics, for example, with surface resistivities ranging from 10 to 106 Ω/□, controllable to within 10%. Avloni says that the textiles have seen some use in piezoresistive-pressure-sensing applications, including a dynamic pressure sensor for biomedical and custom-footwear applications.

Neither the NanoSonic nor the Eeonyx technology changes the fabric properties much, if at all. "You still get the drape and feel of a fabric," Avloni says of Eeontex. The conductive treatments can also be translucent enough to avoid much of a visual impact, though some versions of the Eeonyx-coating formulations are black.

The two nanotech approaches have a downside, too. Metal-rubber textiles and Eeontex are currently available in quantities that many large OEMs would consider developmental. What's more, Eeontex has issues with long-term stability owing to the hydrolysis of polypyrrole when you expose it to heat and humidity. The company recently developed a third-generation product that improves stability by a factor of 20, according to Avloni. And laminate can protect the fabrics. But environmental conditions still represent the chief failure mode for ICPs, and design engineers need to account for them, he acknowledges. "Metal wires have their problems, too," he adds. "If you bend them enough, they'll break."

In many sensing applications, smart fabrics don't likely represent a low-cost alternative to an array of pressure transducers. Yet, even if they aren't the cheapest way to sense pressure, fabric sensors can potentially offer value by bringing more freedom to the design of sensing systems. Fabrics can cover large areas, including civil structures, such as bridges, roads, and buildings. They can conform to a wide variety of surfaces, including a human body in motion. And they may be able to measure large strains. Textronics' Burr notes that elastomeric smart fabrics tolerate repeated elongations.

These fabric attributes may result in the development of other types of unique sensors. Textronics, for example, is working on electro-optical movement sensors for medical-monitoring applications. As Burr explains, these sensors integrate a light source and a photodetector into the fabric. As the fabric stretches and returns to its initial shape, different amounts of light pass through the fabric's woven or knit structure. One application for such an optical sensor would be a garment that monitors a patient's breathing or heart. Textronics also recently introduced a biomonitoring product for the consumer market (**Figure 4**).

She also sees the potential for both optical- and strain-based measurements of movement and vibration. And NanoSonic's Claus reveals that the company has come up with a proprietary chemical sensor based on smart fabrics. He's not ready to disclose much about it, other than to say that it works based on electrochemical reactions of a nanocluster on the fabric surface. EDN

Figure 4 Textronics added a heart-monitor electrode to the lower band of a sports bra.

FOR MORE INFORMATION

Eeonyx
www.eeoynx.com

Elexsen Ltd
www.elektex.com

International Fashion Machines
www.ifmachines.com

NanoSonic Inc
www.nanosonic.com

Textronics Inc
www.textronicsinc.com

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1. ElekTex Reference Design Licensing, http://rbi.ims.ca/4922-562.
2. "Electrostatic Self-Assembly," NanoSonic, www.nanosonic.com/esa/esa.html.

AUTHOR'S BIOGRAPHY

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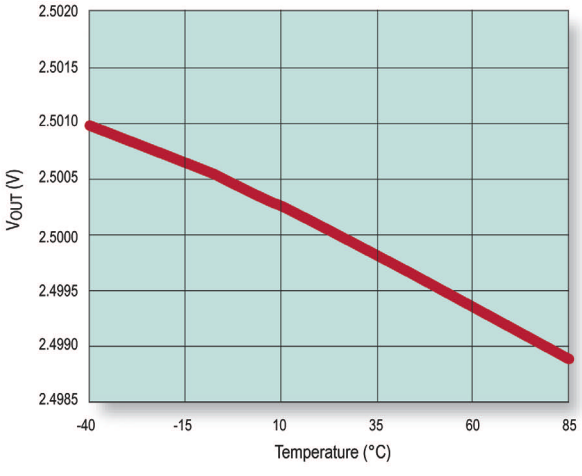

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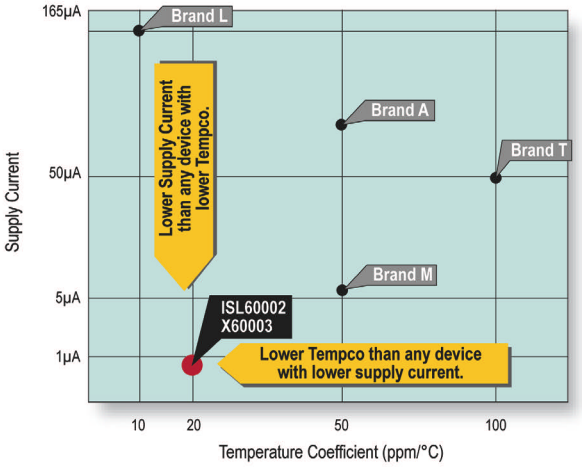

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		C	-2.5		+2.5	mV
		D	-5.0		+5.0	mV
Tempco	-40°C to +85°C				20	ppm/°C
Supply Current	-40°C to +85°C			350	700	nA
Input Range	-40°C to +85°C		2.7		5.5	V
Long Term Drift	ΔTA = 25°C			10		ppm/√1kHrs

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The 33rd Annual Microprocessor Directory

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SEE HOW THE EXPANDED DIRECTORY CAN HELP YOU IN YOUR PURSUIT OF THE PERFECT PROCESSOR FOR YOUR PROJECT.

BY ROBERT CRAVOTTA • TECHNICAL EDITOR

WELCOME TO THE 33RD annual *EDN* Microprocessor/Microcontroller Directory. Successful processor offerings for embedded-application designers stress the optimum balance of processing performance, power consumption, development resources, and bill-of-materials costs. The continuing, growing importance of an optimum balance of application-specific features and peripherals is a focus of this year's update of the directory.

FOR A MORE IN-DEPTH LOOK, VISIT US AT WWW.EDN.COM/MICRODIRECTORY

The number of companies and devices the directory lists continues to evolve, and, once again, we've expanded the company roster and table of devices and cores. The size of the company roster and product listings is a testament to the variety of processors available and the tremendous variation among requirements, features, and types of applications for which designers are using microprocessors and microcontrollers.

Some of the companies newly participating in this year's directory have been selling processor product lines for years but only recently began making them available to the engineering public. Others, such as Luminary Micro, opened their doors for business for the first time during the year. Still others have familiar names but did not participate in last year's directory; we welcome them and look forward to their participation in future updates of the directory.

This directory aims to provide designers and system architects enough visibility into processor options to quickly narrow the list of candidate processors for each project. An expanded online section presents each processor with detailed information and block diagrams. The directory is also adopting a common taxonomy for describing and categorizing target applications. With this first shot at applying the taxonomy, we hope to provide new capabilities for you to quickly find and compare competing processors for your projects. The Web material has more details on the common application taxonomy, so that you can comment on it, and we can refine it, if necessary.

The directory provides a company roster, and it identifies what is new at each company and what applications each company's product lines target. The new "Where are they?" sidebar on the Web helps you find companies that we no longer list, whether because they closed their doors, another company acquired them, or they did not supply us with the information we needed for this year's directory. As always, the Web site duplicates the material you find in the print version.

Our Web site greatly expands on this edition of the Microprocessor Directory. You will find not only the extensive device and core tables, but also dedicated pages for each company's devices, cores, development tools, and other product offerings. These product pages include architectural block diagrams, if available, for each vendor's offerings.

If you cannot find a company in the directory, or it did not participate in the update, please let the company and *EDN* know that you missed reading about it in the directory. Likewise, if this directory helps you find or choose a device or core, please let the vendor know how you found its part. Help us continue to improve the directory by visiting us at www.edn.com/microdirectory or by sending your comments and feedback to mpdirectory@edn.com.

Microprocessor Directory

ACTEL • WWW.ACTEL.COM

Actel offers the CoreMP7, an optimized version of the ARM7 processor core. The processor core is available for use without license fees or royalties when you use it in M7 versions of Actel's flash-based ProASIC3 FPGAs and Actel Fusion PSCs (programmable system chips). The mixed-signal M7 Actel Fusion PSC FPGA family allows designers to integrate support for ±12V analog I/O, as much as 8 Mbits of embedded flash memory, an integrated ADC, and as many as 1.5 million system gates of programmable-logic fabric in a single device.

Actel also offers the Core8051 8-bit-microcontroller IP (intellectual-property) core. The core executes all ASM51 instructions, and it executes instructions in a single cycle. The Core8051 operates as fast as 40 MHz. For as little as 15 cents/MIPS in a single chip, the Core8051 targets consumer, communications, automotive, industrial, and military/aerospace applications.

ADVANCED MICRO DEVICES • WWW.AMD.COM

AMD's (Advanced Micro Devices) x86-based products span the consumer embedded-system market and serve enterprise-class servers and workstations, extending the x86 ISA (instruction-set architecture) across 32- and 64-bit PC, server, and workstation platforms with AMD64 technology. The AMD64-technology-based processors support 64-bit x86 computing for scalable, high-end embedded designs. AMD64 technology leverages x86 hardware and software for embedded implementations for storage, telecommunications, medical, military, and industrial environments.

The AMD Geode processor enables small form factors with optimized x86 performance and reduced power consumption targeting broadband multimedia, set-top boxes, tablet PCs, kiosks, network appliances, and thin-client applications.

ALTERA • WWW.ALTERA.COM

This year, Altera introduced the Nios II C2H (C-to-hardware) acceleration compiler to enable developers to increase the performance of their embedded software. The new tool converts performance-critical C-language subroutines into hardware accelerators and integrates them into FPGA-based Nios II subsystems. The Nios II family of soft embedded processors features a general-purpose, 32-bit RISC CPU architecture in three configurations. The Nios II/f core emphasizes processing performance, the Nios II/e focuses on economy, and the standard Nios II/s is a core configuration that balances performance and core size. The Nios II Embedded Design Suite includes 32-bit, single-precision, IEEE 754-compatible, floating-point support and the Nios II C2H compiler. Designers can add Nios II processors to their systems using the SOPC (system-on-programmable-chip) Builder tool in Altera's Quartus II design software.

The Stratix II GX family is Altera's third-generation of FPGAs with embedded transceivers. With as many as 20 low-power transceivers operating at 622 Mbps to 6.375 Gbps, Stratix II GX FPGAs target application designs with requirements for low power and superior signal integrity for high-speed serial transceivers.

NEW ALTIUM • WWW.ALTIUM.COM

Altium's Altium Designer development system combines board-level hardware, embedded software, and programmable hardware-development tools in a unified environment. It supports device- and vendor-independent electronic-product development using soft, hybrid, and discrete processors. Altium

Designer supports a choice of processor platforms. In addition to facilitating pc-board-system design, it supports interactive FPGA system development. Altium Designer includes a number of royalty-free, 8- and 32-bit, FPGA-based soft processors, including Altium's FPGA-independent TSK3000RISC core, and corresponding software-development-tool sets. You can also use Altium Designer to target development for Nios II and MicroBlaze soft processors, the PowerPC within Xilinx's Virtex-II Pro devices, and discrete ARM7 and PowerPC devices.

ANALOG DEVICES • WWW.ANALOG.COM

In April, Analog Devices added the ADuC7128 to its family of precision analog microcontrollers; it integrates a 12-bit, multichannel ADC with a 32-bit ARM7 processor core. It supports a sampling rate as high as 1M samples/sec, and it includes 126 kbytes of embedded flash memory and analog peripherals targeting motor-control and smart-sensing applications for industrial and automotive-system designs.

Analog Devices' Blackfin processor delivers signal-processing performance and power efficiency with a 32-bit RISC-programming model on an SIMD (single-instruction-multiple-data) architecture. The company announced the availability of four new Blackfin processors: the ASDP-BF538F, ASDP-BF539F, ADSP-BF538, and ADSP-BF539. The ASDP-BF538F and ASDP-BF539F integrate flash memory with a Blackfin core in one package. The BF539 and BF539F processors include CAN (controller-area-network)- and MOST (media-oriented-system-transfer)-bus connectivity targeting the automotive market.

Analog Devices' SHARC (super-Harvard-architecture-computer) processors combine a high-performance fixed- and floating-point processing core with sophisticated memory and I/O-processing subsystems to target high-end audio-processing applications.

APPLIED MICRO CIRCUITS CORP • WWW.AMCC.COM

AMCC (Applied Micro Circuits Corp) offers embedded PowerPC processors targeting control-plane processors, storage, and general-purpose use. The 405 core delivers as many as 600 DMIPS (Dhrystone MIPS), and the 440 core delivers as many as 1600 DMIPS. New products from AMCC include the 440EPx and 440GRx, which include integrated security coprocessors. The 440SP/SPe includes RAID (redundant-array-of-independent-disk) 5 and 6 functions, and the 405EZ includes a new timer feature, as well as IEEE 1588 Ethernet and cellular-RAM support. AMCC PowerPC advantages include leading-edge DRAM support, such as DDR2 SDRAM, high-performance PCI Express, and PCI-X 2.0 I/O interfaces; accelerated Gigabit Ethernet support; and state-of-the-art security.

ARC INTERNATIONAL • WWW.ARC.COM

ARC International offers two configurable, 32-bit processor-core families. The ARC 600 targets battery-operated and cost-sensitive products in the embedded-control, consumer, networking, and automotive markets. The ARC 700 delivers computing performance targeting graphics, media, packet processing, and high-end embedded platforms using operating systems such as Linux.

ARC also offers configurable, multistandard, preverified ARC Video and ARC Sound Advanced subsystems that target portable media devices and advanced-definition audio applications, respectively. The company based the subsystems on an ARC 700 core with a 128-bit SIMD (single-instruction-multiple-data) accelerator; a media-centric DMA engine; and video, imaging, or audio codecs. ARC's SIMD engine powers both subsystems with more than 100 new, 128-bit-wide customized instructions for audio and video processing.

ARM • WWW.ARM.COM

ARM licenses semiconductor IP (intellectual property), including processors, peripherals, interconnect, and physical libraries for the development of complex system-on-chip devices. ARM processors target automotive, consumer-entertainment, imaging, networking, storage, security, and wireless applications. The company based them on a common architecture that emphasizes performance, low power consumption, and reduced system cost. ARM offers a range of processor cores, including the ARM7, ARM9, ARM10, and ARM11 families and the new Cortex family featuring Thumb-2 technology. ARM also offers the SecurCore family, which targets secure applications, such as smart cards and SIMs (subscriber-identity modules), and the OptimoDE (data-engine) signal-processing technology. ARM develops supporting software, including TrustZone technology for data security and DRM (digital-rights management), Jazelle Java-acceleration software, Swerve 3D, and Intelligent Energy Manager.

Over the last year, ARM has focused on delivering new processors to address market applications across the performance spectrum. The new high-performance ARM Cortex-A8 processor targets consumer products running multichannel video, audio, and gaming applications. For next-generation mobile devices, the ARM Cortex-A8 processor delivers performance with a power consumption of less than 300 mW in a 65-nm technology. The new midrange Cortex-R4 processor targets the performance requirements of next-generation embedded products, including mobile phones, hard-disk drives, printers, and automotive controllers. It features an advanced microarchitecture with the ability to issue dual instructions. The ultracompact ARM Cortex-M3 processor targets 32-bit performance for high-volume, cost-sensitive embedded-system applications, such as microcontrollers, automotive-body systems, white goods, and networking devices.

ATMEL • WWW.ATMEL.COM

Atmel supplies flash-microcontroller-based systems targeting consumer, computer/networking, communications, security/smart cards, automotive, industrial, medical, military, and aerospace applications. Atmel offers the AVR , AVR32, ARM7, ARM9, 8051, Teak, and Diopsis DSP cores.

Atmel's AVR microcontrollers include the AVR32, AP7000, and picoPower. The AVR32 32-bit RISC-processor core provides more processing per clock cycle for higher throughput. The AP7000 is the first AVR32-based processor family and the first to integrate on one chip virtually all of the functions multimedia systems require for mobile phones, digital cameras, PDAs, automotive infotainment, set-top boxes, and home-entertainment systems. The picoPower uses a power-saving technology that provides multiyear battery life in lighting control, security, keyless entry, ZigBee, and other applications that spend most of their time in sleep mode.

BROADCOM • WWW.BROADCOM.COM

Broadcom provides a family of high-performance, low-power, integrated processors targeting data-networking and communications applications, as well as security, storage, 3G-wireless infrastructure, and high-density computing. The Broadcom broadband CMP (chip-multiprocessing) systems integrate as many as four 64-bit MIPS processor cores

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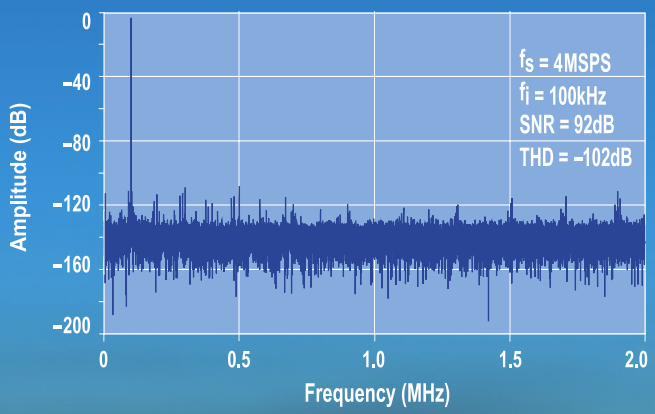

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onto one die. This configuration achieves higher aggregate performance than multiple discrete cores and dramatically reduces board space and power dissipation.

CAMBRIDGE CONSULTANTS
• WWW.CAMBRIDGECONSULTANTS.COM

Cambridge Consultants' XAP3, XAP4, and XAP5 family of RISC-processor soft cores targets low-cost ASIC products with high code density, good performance, low power, and small die. Target applications include mixed-signal wireless, sensors, media, and mobile ASICs in which a design must meet cost and power constraints with the ability to run protocol stacks and an operating system.

The XAP instruction set mixes 16- and 32-bit instructions and targets applications written in C using an RTOS (real-time operating system). The processors support position-independent code, byte addressing, and unaligned data access for software portability and fast access to tightly packed data. They feature protected operating-system modes with register sets for user, supervisor, and interrupt code to provide secure operation when applications misbehave.

Designers can implement the 16-bit XAP4 using as few as 12,000 gates. The 18,000-gate, 16-bit XAP5 processor has a 24-bit address bus that can run programs as large as 16 Mbytes. The 32-bit XAP3 processor has 30,000 gates. An XAP often replaces an older 8- or 16-bit CISC core that requires better performance or in which code has grown too large.

NEW CAST • WWW.CAST-INC.COM

Cast's broad line of IP (intellectual-property) cores includes 8-, 16-, and 32-bit processors. The 8051 cores execute instructions with one clock per cycle. A new configurable 8051 is available in popular variations or with full configurability. Additional cores include 8-bit Z80 and 16-bit 68000 compatible devices.

Cast offers a new series of 32-bit cores targeting deeply embedded systems needing more performance than an 8051. These APS (Advanced Processing Solution) cores require as few as 7000 gates, perform at 0.6 DMIPS (Dhrystone MIPS)/MHz, and use as little as 18 µW/MHz of power. Performance- and code-optimized versions are available, and the devices include a Gnu tool set with JTAG debugging. Partner MicroCross (www.microcross.com) provides an integrated development environment for APS. Integrated APS platforms and design services are available.

CAVIUM NETWORKS
• WWW.CAVIUM.COM

Cavium Networks offers security and MIPS-based single-core and multicore processors for networking, wireless, storage, and control-plane applications. Cavium Networks offers a portfolio of integrated, software-compatible processors and accelerator boards ranging in performance from 10 Mbps to 10 Gbps that enable secure, intelligent functionality in SOHO (small-office/home-office)/SME (small-to-midsized-enterprise) and enterprise- and service-provider network equipment. The company's processors are supported by software, silicon, and ODM (original-design-manufacturer) hardware offerings from leading vendors in networking, UTM (unified-threat-management), wireless, voice, operating systems, Java, and motherboards.

Cavium Networks' MIPS-based family of broadband-communication processors includes Nitrox SOHO and Octeon CN30XX products. These products provide leading integration and price/performance for SOHO/SME equipment and control-plane applications from 10 Mbps to 1 Gbps. The multicore Octeon MIPS64 family of processors includes one to 16 cnMIPS cores on a single chip, along with advanced networking, security, and application-hardware acceleration. The cnMIPS core is Cavium's custom implementation of MIPS64 Release 2 for networking and services requiring low power. The Octeon processor family supports scalability in a compatible manner from 200 Mbps to more than 10 Gbps of network-application performance.

CIRRUS LOGIC
• WWW.CIRRUS.COM

Cirrus Logic supplies high-precision analog, mixed-signal, and embedded processors for the audio and industrial markets. In the general-purpose-processor segment, Cirrus Logic offers highly integrated ARM9- and ARM7-based embedded processors targeting industrial and networked consumer applications. These embedded processors support Linux and WinCE. Developers can leverage Cirrus Logic's two proprietary technologies, MaverickKey and MaverickCrunch, for DRM (digital-rights management) and math coprocessing.

Cirrus Logic's NineSeries of ARM9-based products includes the EP9301, EP9302, EP9307, EP9312, and flagship EP9315. The entry-level EP9301 integrates Ethernet and two USB 2.0 host ports, and the EP9302 adds MaverickCrunch and MaverickKey to go along with increased processing power and memory. The EP9307 adds a graphics accelerator, touchscreen and keypad support, and three USB ports. The EP9312 integrates an IDE (integrated development environment) and support for high-quality audio. The flagship EP9315 adds support for the PCMCIA interface.

NEW CLEARSPEED
• WWW.CLEARSPEED.COM

ClearSpeed Technology, a specialist semiconductor company, focuses on delivering high-performance coprocessors for use alongside general-purpose processors in computationally intensive applications. ClearSpeed's advanced, multithreaded-array-processing technology lets designers accelerate data-intensive applications at low power. Products include chips, boards, software tools, applications, and support.

The power-efficient ClearSpeed CSX600 embedded parallel processor has 96 cores that execute as many as 25 64-bit GFLOPS and averages less than 10W of energy consumption.

CRADLE TECHNOLOGIES
• WWW.CRADLE.COM

Cradle's CT3600 family of scalable MDSP (multicore-DSP) processors integrates multiple general-purpose processors with multiple DSPs to improve processor efficiency for control code and computationally intensive media-processing algorithms. Targeting media-processing applications, particularly those involving complex, intelligent-video applications, the CT3600 family comprises two products containing eight to 16 DSPs on a single chip. The largest version, with 16 DSPs and eight general-purpose processors, operates at 350 MHz, supports 16 channels of CIF (common-intermediate-format)-resolution Simple Profile MPEG-4 encoding, and can perform more than 22,000 16-bit MACs (multiply-accumulate operations)/sec, quadrupling the total performance over Cradle's previous-generation MDSP.

The CT3600 architecture includes an intelligent, three-tier-memory hierarchy that minimizes external-memory-access stalls; a wide and flexible DDR SDRAM interface; a high-performance, 64-bit internal global bus; and several dedicated I/O and DRAM DMA engines to meet the high-throughput requirements of computationally intensive audio- and video-processing applications. A smart I/O subsystem provides as many as

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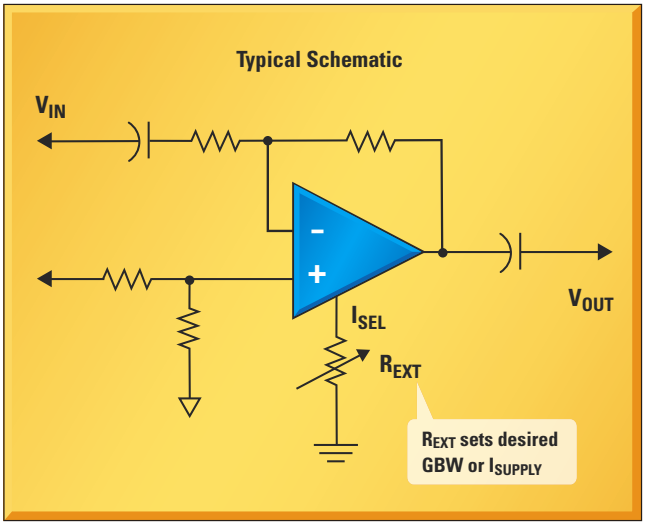

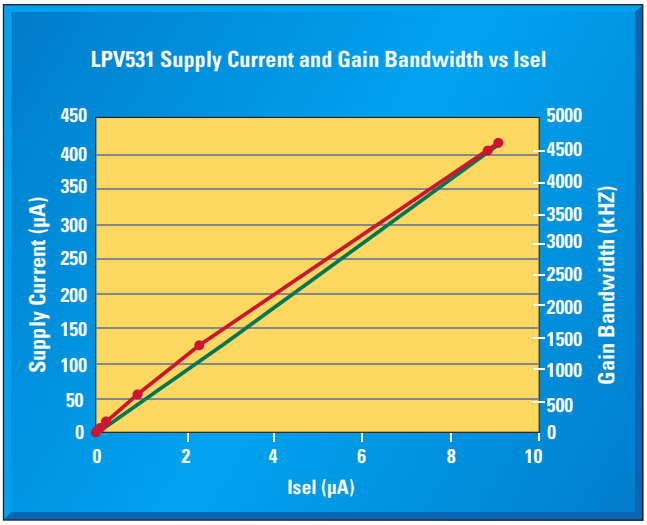

Product ID	No. of Channel	Typical Supply Current per Channel (mA)	Supply Voltage Range (V)	Input Offset Voltage (mV)	RRI/O	Unity Gain Bandwidth (MHz)	Low Input Current CMOS Design	Feature	Temp Range
LMP7711/12	S/D	1.15	1.8 to 5.5	0.15	RRO	17	✓	Shutdown	Ext
LMP7715/16	S/D	1.15	1.8 to 5.5	0.15	RRO	17	✓	—	Ext
LMP7701/04	S/Q	0.72	2.7 to 12	0.2	RRI/O	2.5	✓	—	Ext
LMV791/792	S/D	0.95	1.8 to 5.5	1.3	RRO	14	✓	Shutdown	Ext
LMV796/797	S/D	0.95	1.8 to 5.5	1.3	RRO	14	✓	—	Ext
LMV651/654	S/Q	0.11	2.7 to 5.5	1.5	RRO	12	—	—	Ext
LPV531	S	Program	2.7 to 5.5	3.5	RRI/O	Program	—	Stand-by	Ind
LPV511	S	880 nA	2.7 to 12	3	RRI/O	0.027	—	—	Ind

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CYAN TECHNOLOGY
• WWW.CYANTECHNOLOGY.COM

Cyan Technology did not provide an update to this year's directory. The company's low-power, 16-bit, embedded-communications, flash-based eCOG1k microcontroller implements a 25-MHz RISC Harvard architecture that includes internal flash memory, RAM, and cache. The external-memory interface supports addressability of 32 Mbytes of external memory. Additional features include a smart-card interface, a 12-bit ADC, a temperature sensor, and a proprietary-port configurator. Cyan's CyanIDE development software includes a full ANSI unlimited-C compiler, simulator, debugger, and peripheral-configuration software. Users can select those peripherals they need and connect them to a choice of pins. The peripheral-register-setup code automatically generates in assembly language. All Cyan development software is downloadable and free.

CYBERNETIC MICRO SYSTEMS
• WWW.CONTROLCHIPS.COM

Cybernetic Micro Systems did not provide an update to this year's directory. The company produces a line of ASICs to interface to a variety of peripherals that would be difficult to control from a general-purpose computer. These chips provide a programmable interface to the low-level functions of the peripheral. The 100-pin, 8-bit P-51 microcontroller either sits between the host computer and the peripheral device or becomes the peripheral device.

CYPRESS MICROSYSTEMS
• WWW.CYPRESSMICRO.COM

Cypress's system-level PSoC (programmable-system-on-chip) mixed-signal array has configurable digital and analog peripherals, an 8-bit microcontroller, and three types of embedded memory. PSoC target applications include automotive, communications, computers and peripherals, consumer, industrial, mobile/wireless, motor control, and security.

PSoC integrates as many as 12 analog and 16 digital configurable hardware blocks in a single device. PSoC blocks can implement a variety of user-selectable hardware-peripheral functions that you configure through register settings. The analog blocks encompass an operational amplifier and include programmable multiplexing and feedback characteristics. Each digital block is an 8-bit-wide resource; therefore, creating an 8-bit PWM requires one digital PSoC block. You can use two or more blocks together to create wider bit functions.

DALLAS SEMICONDUCTOR/ MAXIM INTEGRATED PRODUCTS
• WWW.MAXIM-IC.COM

Dallas Semiconductor offers four microcontroller families targeting networked, secure, mixed-signal, and 8051 drop-in designs. The network microcontrollers provide low-cost connections for networking applications and optionally include a complete TCP/IP (Transfer Control Protocol/Internet Protocol) network stack in ROM, a built-in Ethernet MAC (media-access controller), CAN (controller-area network), and parallel and serial ports. The devices use a four-clock-per-machine-cycle 8051 core operating as fast as 75 MHz with an extended 22-bit addressing range and 16 Mbytes of direct addressing.

The secure microcontrollers target applications demanding protective measures against theft of proprietary or secret information. These devices employ encryption and physical-protection techniques that support point-of-sale terminals, automated teller machines, banking, and gaming equipment. The mixed-signal microcontrollers feature high-performance, low-power, 8- and 16-bit RISC cores with analog peripherals.

DIGI INTERNATIONAL
• WWW.DIGI.COM

Digi based its net-centric NetSilicon Net+ARM processor SOCs (systems on chips) on ARM7 and ARM9 cores. The NS9360, NS9750, and NS9775 employ the ARM926EJ-S core. The NS9360 operates at 177 MHz and integrates 10/100-Mbps Ethernet, USB, an LCD, IEEE 1284, and serial I/O. The NS9750 operates at 100 MHz and includes all of the NS9360 features, plus PCI support. The high-performance NS9775 color-laser-printer processor operates at 200 MHz and integrates 10/100-Mbps Ethernet, USB, and PCI to improve the cost performance of color laser printers. Digi based the NS7520 on the ARM7TDMI core. It operates at 55 MHz and integrates 10/100-Mbps Ethernet, serial I/O, and a general-purpose interface.

EM MICROELECTRONIC
• WWW.EMMICRO ELECTRONIC.COM

EM Microelectronic specializes in ultralow-power, low-voltage ICs for battery-operated and field-powered applications in consumer, automotive, and industrial areas. Product offerings include ROM or flash memory, as many as four multiplexer LCD drivers, RC and crystal oscillators, EEPROM, an ADC, and high-drive outputs. Target applications include temperature-monitoring power supplies; heating, ventilation, and air conditioning; insulin pumps; security; computer peripherals; and RFID tags for animal and retail applications.

This year, EM Microelectronic introduced the EM6682, which operates with a single 1.5V battery. The compact EM6682 features an operating-voltage range of 0.9 to 5.5V, making it suitable for applications such as battery-powered toys, household appliances, and body-care products without the use of additional external components.

FREESCALE SEMICONDUCTOR
• WWW.FREESCALE.COM

Freescale Semiconductor offers microcontrollers, embedded processors, sensors, and analog/power management for automotive, industrial, and consumer applications. Freescale extended its controller continuum with the ultralow-end, RS08-based, 8-bit microcontrollers and an advanced 32-bit ColdFire core for easy migration between 8- and 32-bit architectures. The company expanded its ColdFire portfolio with a Linux kernel, IEEE 802.15.4-protocol support, USB On-The-Go, and Ethernet flash-based controllers. The automotive line includes additions to controllers employing the S08, S12X, and PowerPC cores, as well as FlexRay-ready solutions.

Freescale based its PowerQuicc communications processors on PowerPC cores, and they provide data- and control-plane processing for wireless and wire-line infrastructure, enterprise networking, home and SOHO (small-office/home-office) networking, and pervasive computing. Freescale offers application-specific PowerQuicc III devices, delivering gigahertz-class performance, and comprehensive reference platforms employing PowerQuicc II Pro processors to target consumer and small-office designs. Freescale's high-performance PowerPC processors, including the MPC7448 and advanced MPC8641D dual-core device, support communications applications.

Freescale based its i.MX application processors on ARM-core technology. They target multimedia applications in wireless handheld devices for the home and car. The processors employ Smart Speed technology that balances multimedia performance with battery life.

AUTOMOTIVE EMBEDDED SEMICONDUCTOR SOLUTIONS

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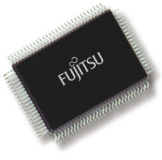

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• WWW.FMA.FUJITSU.COM

Fujitsu's 32-, 16-, and 8-bit microcontrollers include general-purpose and application-specific versions; most of the microcontrollers include onboard-flash, ROM, ADC, DAC, CAN (controller-area-network), USB, and LCD controllers to target automotive, communications, computer-peripheral, industrial, and consumer applications. A full complement of software- and hardware-development tools supports these microcontrollers. The F2MC (Fujitsu flexible microcontrollers) line includes the 8-bit F2MC-8L and F2MC-8FX series and the 16-bit F2MC-16L/16LX/16F series. The FR (Fujitsu RISC) integrates as much as 768 kbytes of internal flash; ROM; as much as 160 kbytes of internal RAM; an external-bus interface; an ADC; a DAC; and multiple CAN, LIN (local-interconnect-network), USB, UART, SIO, and I^2C interfaces. The series also has a stepper motor and LCD controllers for auto, communications, computer-peripheral, industrial, consumer, and security applications.

HYPERSTONE

• WWW.HYPERSTONE.COM

This year, Hyperstone introduces a cost-effective processor that the company based on a core similar to the E1-32XSRU RISC/DSP. The E1-32XSIO processor targets cost-sensitive applications requiring RISC/DSP code and fast serial communications. Hyperstone's hardware/software-development package and libraries include communication stacks, a real-time kernel, and extensive DSP functions.

Additionally this year, Hyperstone offers the S4 SD/MMC (multimedia-card) flash-memory controller and the U2 SD/MMC/USB flash-memory controller. These controllers support the SD 1.1, MMC 4.0, and USB 2.0 specifications. The devices can achieve 18-Mbyte/sec-read and 15-Mbyte/sec-write speeds. You can use them to produce SD and MMC cards, as well as USB 2.0 flash-disk drives or combination devices.

NEW IBM TECHNOLOGY COLLABORATION SOLUTIONS

• WWW.IBM.COM

IBM Technology Collaboration Solutions offers embedded microprocessor cores and microprocessors employing the open Power Architecture technology. IBM's offerings include the fully synthesizable, 32-bit PowerPC 405 and 440 embedded cores, along with 32- and 64-bit families of power- and performance-optimized microprocessors. Targeting consumer, networking, communications, imaging, industrial, data-processing, and storage applications, IBM's 405 and 440 embedded cores offer scalable performance for custom-SOC (system-on-chip) integration. Developers can license these cores from IBM for use in client-specific designs and at any manufacturer.

IBM's 750 family of 32-bit microprocessors targets consumer designs, including printers, communications, storage, and data-processing applications. The 750 series features superior reliability and extended product lifetimes and can meet the demands of cost-sensitive, high-performance, and power-conscious applications. The 970 series of microprocessors offers a performance-driven 64-bit architecture with native 32-bit application compatibility. Targeting computationally intensive and bandwidth-intensive applications, IBM's 970 family includes recently announced low-power and dual-core offerings.

NEW IMSYS TECHNOLOGIES

• WWW.IMSYSTECH.COM

Fabless-semiconductor company Imsys is in Stockholm, Sweden, with US offices in Sunnyvale, CA, and Dallas. The company develops reconfigurable-processor platforms. You can program the processors in Java, C/C++, assembler, and microcode. An important part of the company offering is the Internet-enabled reference modules that IBM ships as ready-to-go subsystems with complete operating-system and file-system environments. The integrated hardware and software platform targets wired and wireless communications, graphics-display technologies, and image processing in telecom, automotives, industrial automation, and consumer electronics.

INFINEON TECHNOLOGIES

• WWW.INFINEON.COM

This year, Infineon introduced 32-bit microcontrollers for industrial-motor-control applications, a family of 16-bit microcontrollers for industrial and automotive applications, and a new 8-bit series with integrated network connectivity.

The six new 32-bit TC116x series of TriCore microcontrollers employ a unified microcomputer/DSP architecture that operates as a single multitasking engine with fast context switching. Higher performance system designs can use the 80-MHz TC1163/64, with 1 Mbyte of flash and an onboard peripheral-control processor, or the TC1165/66 with 1.5 Mbytes of flash.

Infineon based the XC164CM series on the 16-bit XC166 architecture. It offers 25-nsec DSP-instruction execution, integrated peripherals, an intelligent PWM unit, and 32 or 64 kbytes of flash memory. A high-speed, 14-channel ADC accommodates complex analog data transforms, and a TwinCAN module and extended serial interfaces provide network connectivity.

The 8-bit XC886/888 microcontrollers offer an integrated CAN controller and LIN (local-interconnect-network) support.

INTEGRATED DEVICE TECHNOLOGY • WWW.IDT.COM

The IDT Interprise family of integrated communications processors delivers data processing at line-rate speed with processing headroom for value-added features. IDT based the processor cores on the 32-bit MIPS ISA (instruction-set architecture). Interprise processors and their associated system-development tools target designs for SOHO (small-office/home-office) routers, Ethernet switches, WAPs (wireless-access points), and VPN (virtual-private-network) equipment.

INFRANT TECHNOLOGIES

• WWW.INFRANT.COM

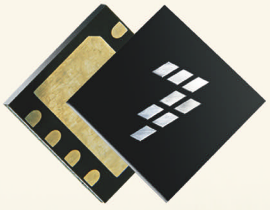
Infrant did not provide an update to this year's directory. The company's highly integrated NSPs (network-storage processors) target NAS (network-attached-storage) and media-server-appliance applications. The NSPs enable efficient network-storage devices by integrating Gigabit Ethernet, multiple Serial ATA hard-disk interfaces, and hardware-based RAID (redundant-array-of-inexpensive-disk) 0/1/5 redundancy into a single device.

Infrant's second-generation NSPs, the IT3102 and IT3107, target the home-media-server and SOHO (small-office/home-office) NAS markets.

INTEL • WWW.INTEL.COM

The dual-core, low-voltage, 2-GHz Intel Xeon processor combines the benefits of two high-performance execution cores with intelligent power-management features to deliver significantly greater performance per watt than previous single-core Intel Xeon-processor-based platforms. The dual-core/dual-processor capabilities target low-power communications and embedded-system applications.

The IXP460 and IXP465 network processors offer a higher speed Intel XScale core,



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expanded connectivity options, and enhancements to improve end-system reliability and security. The IXP2325 and IXP2350 network processors target network access and edge applications by combining data- and control-plane processing capabilities in a single chip.

INTELLASYS
• WWW.INTELLASYS.NET

IntellaSys based its multicore chips on the proprietary SEA (Scalable Embedded Array) Platform, which uses a dual-stack architecture that is both asynchronous and scalable. The inaugural SEAforth-24 family packs a 6×4-processor array of 18-bit processors, each of which can operate at 1 BOPS.

As a RISC version of Forth software, the VentureForth programming language deploys 32 instructions, including full 18×18-bit multiplies with 36-bit results. VentureForth enables compact code, and it makes the SEA of processors possible by providing a software basis for dozens or hundreds of cores. Each core runs independently of the others and at the full native speed of the silicon.

IPFLEX
• WWW.IPFLEX.COM/EN/

IPFlex offers dynamically reconfigurable processors and design-tool platforms targeting industrial-image-processing, network-security, and scientific-computing applications. The DAPDNA (digital-application-processor/distributed-network-architecture) series of processors incorporate a RISC processor as a controller and a heterogeneous matrix of 300 to 1000 16- to 32-bit processing elements that the system can reconfigure in a single clock cycle.

The design-tool suite includes a Data Flow C compiler that IPFlex jointly developed with Celoxica (www.celoxica.com). The compiler enables designers to describe algorithms in a C-like syntax, which is partly based on Handel-C, and automatically generates hardware code.

IPFlex expects that DAPDNA-2 and DAPDNA-IMS processors will find use in image-inspection systems, network security, and multifunction-printer applications.

LATTICE SEMICONDUCTOR
• WWW.LATTICESEMI.COM

The LatticeMico8 is an 8-bit soft microcontroller core with an 18-bit-wide instruction set and 32 general-purpose registers. Targeting use in Lattice devices, the LatticeMico8 microcontroller consumes fewer than 200 LUTs (look-up tables) in the smallest configuration. You can get a license for the LatticeMico8 under an open IP (intellectual-property)-core license agreement that you can download from the Lattice Web site. The license preserves the open nature of the core by permitting use alongside proprietary designs and allows hardware implementation and distribution without the need for a license agreement. In addition to the core design in Verilog and VHDL, Lattice also provides an assembler and an instruction-set simulator, both as source code under the standard GNU GPL (general-public-license) agreement.

LUMINARY MICRO
• WWW.LUMINARYMICRO.COM

Luminary Micro designs, markets, and sells ARM Cortex-M3-based microcontrollers for embedded and industrial applications. The Austin, TX, company's new Stellaris family is the first silicon implementation of the Cortex-M3 microcontroller core. The leading entry-level product in the Stellaris family is the first 32-bit ARM-based processor available for $1. This 20-MHz microcontroller targets 8- and 16-bit-microcontroller applications by enabling developers to enter the ARM architecture for a similar price as 8- and 16-bit devices.

Luminary Micro also introduced four 32-bit microcontrollers that include more onboard memory, ADC functions, and a sophisticated motion-control unit. These features target algorithmically intensive high-end applications, such as digital industrial controllers and brushless dc motors, which find use in products for industrial automation and instrumentation and robotics.

MICROCHIP TECHNOLOGY
• WWW.MICROCHIP.COM

Microchip offers both 8- and 16-bit PIC microcontrollers, as well as 16-bit dsPIC DSCs (digital-signal controllers). The company based its 8-bit PIC microcontrollers on a RISC-core architecture that enables designers to migrate from six- to 100-pin devices among all families with little or no code changes. Features include sophisticated timing peripherals, integrated ADCs, communications peripherals, and in-circuit serial programming. Memory options include PEEC (PMOS-electrically-erasable-cell) flash, which can provide 1 million erase/write cycles on each memory location at a wide range of operating temperatures; EEPROM; OTP (one-time-programmable) memory; and ROM.

The 16-bit PIC24 microcontrollers offer as much as 40-MIPS performance and provide high throughput and efficient C-code density. The PIC24F family offers a cost-effective step up in performance, memory, and peripherals for many applications that are pushing the envelope of 8-bit-microcontroller capabilities. For more demanding applications, the PIC24H offers 40-MIPS performance, more memory, and additional peripherals, such as CAN (controller-area-network) communication modules.

Microchip also offers two 16-bit dsPIC DSC families that provide compatible DSP options across a spectrum of prices, performance, and features. Common attributes among all of Microchip's 16-bit microcontroller and DSC families are pinout, software, and peripheral compatibility and common development tools.

Major introductions from Microchip this year included several 8-bit microcontrollers and development tools that provide general-purpose building blocks for electronic systems.

MIPS TECHNOLOGIES
• WWW.MIPS.COM

MIPS Technologies offers embedded-processor architectures and cores targeting digital consumer, networking, personal-entertainment, communications, and business applications. The company licenses its 32- and 64-bit RISC IP (intellectual property) to semiconductor companies, ASIC developers, and system OEMs. Industry-standard tools, software, and services support the MIPS architecture.

The flexible synthesizable processors range from the M4K core with 30,000 gates to the high-performance, multithreaded 34K family with 34,000 gates. The MIPS32 34K family of cores is the first to integrate the MIPS MT (multithreaded) ASE (application-specific extension). The architecture improves processing throughput by feeding additional threads into the pipeline as one thread stalls for memory accesses.

NATIONAL SEMICONDUCTOR
• WWW.NATIONAL.COM

National Semiconductor's CP3000 connectivity-processor family combines a RISC core with on-chip SRAM and flash memory, hardware-communications peripherals, and an expandable external bus to target embedded-system-communications applications, such as automotive telematics, vehicle-network gateways, hands-free car kits, and industrial- and medical-instrumentation and control. National Semiconductor's single-chip CP3000 processors feature a high-

LXI delivers real benefits now, Plus flexibility for the future

With its LXI products, Agilent Technologies offers engineers cost efficiency, performance and ease of operation

LXI is probably the biggest news to hit the instruments business in a generation. It promises across-the-board improvements in just about everything from performance, to cost, to ease of deployment.

What makes LXI different? Economies of scale, for one thing. The LXI standard (LAN eXtensions for Instrumentation) is based on the most widely used local area network (LAN) technology, Ethernet. And Ethernet is the universal language of networking. Millions of engineers are already familiar with it, and it continues to improve, boasting speeds of up to 10 Gbits per second over copper wires.

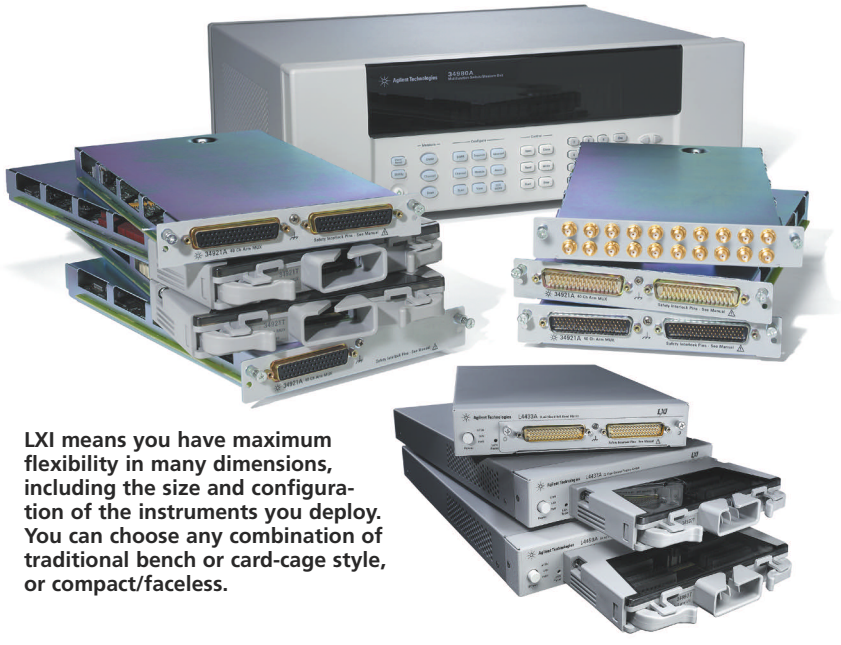
LXI's roots in Ethernet mean you can count on automatic speed upgrades as commercial products continue to evolve. Furthermore, by building on standard technologies, industry experts predict that LXI-based instruments will be comparatively inexpensive, yet have a richer set of features and functionality.

But beyond those many strategic architectural advantages, LXI offers a large number of compelling and immediate benefits — benefits that can have a direct impact on costs, implementation goals, and ease of operation.

Off to a quick start

For instance, right from the start, LXI is easier to set up than card cage systems and older, proprietary interfaces. There's just less to think about. The connections and interfaces are simpler. And there's less of a requirement for specialized knowledge. That translates into faster and cheaper implementation. Almost every major test & measurement supplier is participating in the development of LXI. This broad participation, combined with the technology's simplicity, mean LXI-based products are easier to integrate. That doesn't just apply to new systems. LXI is also oriented toward backward compatibility, and tools available from vendors such as Agilent Technologies ensure that this compatibility is as extensive as possible.

At the same time, LXI reduces overhead costs because it doesn't require a card cage, or a slot-zero controller. Nor does it demand proprietary interface cards and complex cabling. Instead, it's essentially "plug-and-play" because it leverages the available LAN port that is standard on almost all PCs. All that's needed is a LAN cable or a switch if multiple instruments are involved.



LXI means you have maximum flexibility in many dimensions, including the size and configuration of the instruments you deploy. You can choose any combination of traditional bench or card-cage style, or compact/faceless.

Size doesn't matter

Similarly, LXI instruments can be deployed in any size or form factor, ranging from the classic bench "box" to faceless instruments, suited to compact or rugged duty applications in manufacturing or defense. Additionally, engineers can deploy sensors, amplifiers, filters, and attenuators in remote locations, such as in test fixtures.

Because LXI is based on familiar standards, you can take advantage of almost every kind of communication medium. In environments where large amounts of RF are being generated, you can rely on optical cable. Or, where hard wiring is too expensive or difficult, you can use wireless. The result is that instrumentation difficul-

ties are less of a gating factor for whatever you are trying to accomplish.

For multiple instrument systems, LXI provides optional trigger standards that support easy and accurate synchronization of multiple devices, even if they are physically located miles apart. Indeed, you can set up tight synchronization over a wired LXI trigger bus that is functionally equivalent to a VXI or PXI backplane interconnection. The IEEE 1588 standard built into LXI enables instruments to share a common sense of time. So you can now implement start actions without a specific trigger requirement; synchronize instruments running at different rates; better correlate data; and, more easily troubleshoot both processes and instrumentation. LXI also enables direct communication between instruments, allowing you to minimize wait states in your programs and offload the PC.

Make the connection

In short, LXI delivers the best of all worlds. Standard LAN components are inexpensive, so there are minimal infrastructure costs. LXI performance generally matches or exceeds previously available technology, and data throughput is tremendous, clocking in at 125 times the speed of GPIB. But above all, LXI offers flexibility. You can use as many instruments as desired, put them anywhere in the world, and trigger them precisely.

All this means that LXI is your path to the future, without undermining the investments you have already made. ■

FOR MORE INFORMATION

To learn more about LXI and products that incorporate it, contact:

Agilent Technologies
1-800-829-4444,
www.agilent.com/find/tm-lxi

Agilent's LXI products are part of the Agilent Open Program.
For more information, download the Agilent Open brochure at:
www.agilent.com/find/open

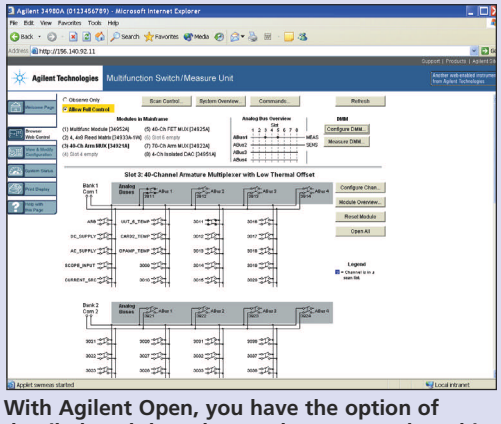
LXI Done Right

A test system isn't what you need to worry about. Your product is. To make LXI test system development and operation more efficient and cost-effective, Agilent has developed Agilent Open, a program that simplifies test-system setup and integration with a versatile combination of test-system hardware, I/O, and software tools.

Agilent Open accelerates the creation of robust test systems that are easy to enhance and maintain by ensuring greater choice in measurements, connectivity and programming. This gives your team more time to focus on what matters most — the performance and reliability of your product.

The Agilent Open approach provides you with the ability to work within a choice of software development environments. For instance, IVI drivers available from Agilent work in all the most widely-used languages (Visual C++, Visual Basic, C#, and J#, as well as VEE Pro, Basic, LabVIEW and LabWindows CVI). Agilent Open also offers many other benefits:

- A rich web interface that goes beyond the functionality required by the LXI standard to support both monitoring and control.
- Software tools like the IO Libraries Suite that significantly reduces the time to set up your test environment, including connectivity tools across any common interface.
- Multiple interfaces and converters, such as LAN, USB and GPIB for general purpose instruments.
- Software tools to make it easier to use your test environment, including tools for the most common Microsoft environment (.NET).
- System ready instruments optimized for speed and ease of integration.



With Agilent Open, you have the option of detailed, web-based "anywhere" control. In this example, you can control the switch matrix simply by clicking on the matrix crosspoints.

And LXI from Agilent delivers real world benefits. For instance, a major automotive component manufacturer needed to improve the testing throughput for electronic control units (ECUs). The application demanded many changes to the bias voltage levels during testing, requiring the power supply to transition quickly to various voltages levels.

By adopting an LXI-compliant, Agilent Open N6700 modular power supply, the company was able to reduce test time from 20 seconds to 17 seconds, a 15% reduction for every device under test. This had an immediate impact on process throughput, saving time and money.

For more information about Agilent Open, go to www.agilent.com/find/open.

Intersil Linear Regulators

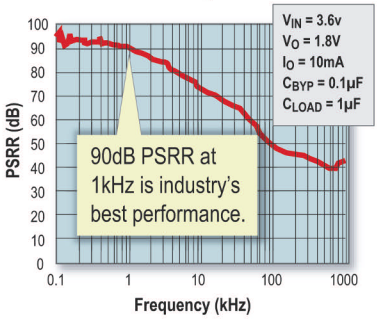
High Performance Analog

Shhhhhhh... We're Trying to Focus Here

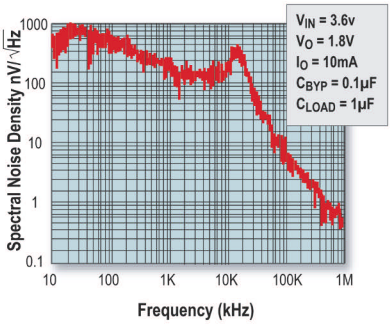
Intersil's new family of Low Dropout Regulators provide the **industry's best PSRR (Power Supply Rejection Ratio) for superior noise performance AND ultra low I_Q.** With this combination, digital images on your RF/noise sensitive applications just got a whole lot clearer.

As digital still cameras and cell phone camera modules move toward higher megapixel resolutions, the need for superior PSRR becomes more critical. With a PSRR of 90dB, low I_Q, and a 3mm x 3mm solution size, Intersil's ISL9000 is the LDO you've been waiting for.

ISL9000 PSRR (POWER SUPPLY REJECTION RATIO) vs FREQUENCY



ISL9000 SPECTRAL NOISE DENSITY vs FREQUENCY



ISL9000 Key Features:

- Very high PSRR: 90dB @ 1kHz
- Extremely low quiescent current: 42µA (both LDOs active)
- Low output noise: typically 30µVrms @ 100µA (1.5V)
- Low dropout voltage: typically 200mV @ 300mA
- Wide input voltage of 2.3V - 6.5V
- Integrates two 300mA high performance LDOs
- ±1.8% accuracy over all operating conditions
- Stable with 1-10µF ceramic capacitors
- Separate enable and POR pins for each LDO
- Available in tiny 10-ld 3mm x 3mm DFN package

Low Dropout Regulator Selection Table

	PSRR at 1kHz	Output Noise Vrms @ 100µA (1.5V)	$I_{OUT}1$ (max) mA	$I_{OUT}2$ (max) mA	I_Q (typ) µA	Voltage Accuracy
ISL9000	90dB	30µ	300	300	42	1.8%
ISL9007	75dB	30µ	400	-	50	1.8%
ISL9011	70dB	30µ	150	300	45	1.8%
ISL9012	70dB	30µ	150	300	45	1.8%
ISL9014	70dB	30µ	300	300	45	1.8%

Datasheet, samples, and more info available at **www.intersil.com**

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performance RISC core, DSP, Bluetooth-lower-link controller, USB 2.0 OTG (On the Go), CAN (controller-area network), Access.bus, Microwire/SPI, ADC, audio-codec, I²S, and Advanced Audio interfaces.

The COP8 flash microcontrollers feature an 8-bit core and as much as 32 kbytes of onboard flash that you can use as data or program storage and that work for more than 100,000 delete/write cycles. The devices offer virtual-EEPROM functions, in-system programming, and integrated analog- and mixed-signal functions for stand-alone and Internet-controlled applications.

NEC ELECTRONICS AMERICA
• WWW.AM.NECEL.COM

NEC Electronics America manufactures and markets highly integrated, low-power embedded microprocessors and microcontrollers, with both embedded flash memory and mask ROM. The 8-bit K0 and K0S families provide low power consumption and integrate peripherals, such as LCD drivers and controllers, for consumer appliances, home health care, building-management systems, and industrial-controlled applications. The new 8-bit 78K0/Lx2 series provides power consumption of 2.5 mA; in-application self-programming memory; and a variety of memory, packaging, and peripheral options.

The V850 family delivers 32-bit-processing performance, low-voltage operation, DSP functions, and on-chip peripherals for consumer-electronics and other embedded-system applications. Recently, the company introduced three additions to the 32-bit V850 series: the V850ES/Hx2, V850ES/Jx2, and V850ES/Kx2. These series provide complex, multifunctional, high-speed operation and a wide range of voltage requirements for security systems, industry equipment, digital consumer electronics, and sensors.

This year, NEC Electronics America announced the 32-bit V850ES/Sx3 and V850E/Dx3 series, which provide peripherals targeting automotive audio control, as well as dashboard- and driver-information applications. NEC Electronics based the devices on the V850ES CPU core, and they share a common architecture to ensure compatibility among software, software-development tools, and system-testing tools. The company expanded its motor-control ASSP (application-specific-standard-product) line with the new 8-bit µPD78F0711 and µPD78F0712 flash-based microcontrollers, which the company based on the 78K0 core, and a new 32-bit flash-based V850ES/IE2 series.

OKI SEMICONDUCTOR
• WWW.OKISEMI.COM/US

Oki Semiconductor did not provide an update to this year's directory. The company's Advantage microcontroller family comprises ARM-core-based products ranging from the ML671000 with a built-in USB controller to the high-performance, 120-MHz ARM946E-based 6200 series with instruction and data caches. Oki's 4060, 4050, 675K, and 674K series ARM7 Advantage microcontrollers offer variations in frequencies, memory sizes, caches, features, and packages.

PHILIPS SEMICONDUCTORS
• WWW.SEMICONDUCTORS.PHILIPS.COM

Philips Semiconductors offers 8-, 16-, and 32-bit devices targeting low- to high-end applications in the consumer, communications, computing, medical, connectivity, and automotive industries. Philips based its latest offering, the LPC3000 family of microcontrollers, on the Nexperia platform. The 90-nm, ARM9-family-based, 32-bit LPC3000 family runs at 1V at speeds as high as 200 MHz. It features a USB, a real-time clock, a NAND-flash interface, Ethernet, and a vector floating-point coprocessor for full support of single- and double-precision calculations.

PMC-SIERRA
• WWW.PMC-SIERRA.COM

PMC-Sierra's MIPS-based processors target metropolitan-transportation, storage-area-networking, wireless-equipment, VOIP (voice-over-Internet Protocol), Internet-routing-equipment, enterprise-switch, and multifunction- and laser-printer applications. The company's family of 64-bit, integrated, 1-GHz CPUs delivers high performance, low latency, and low power consumption with integrated standard interfaces, including PCI, DDR and a DDR memory controller, Gigabit Ethernet, and HyperTransport. The family includes pin-compatible devices that operate at 250 to 900 MHz to support performance scalability.

The MSP (multiservice-processor) family targets CPE (customer-premises equipment), such as wired and wireless VOIP-terminal adapters, home gateways, voice-enabled routers, and NAS (network-attached storage). The open-source-based platform enables third-party vendors to offer enhancements such as VOIP security, advanced QOS (quality of service), and advanced telephony features.

The newest members of PMC-Sierra's MSP family are the MSP8520, MSP7100, and MSP220x. The MSP8520 incorporates a scalable, 600-MHz to 1-GHz E9000 MIPS-based processor with integrated hardware security for storage applications, VPN (virtual-private-network) security appliances, printer and imaging systems, and routers and switches. The multithreaded MSP7100 processors are MIPS32 systems. The MSP220x processors target residential and SOHO (small-office/home-office) NAS applications and integrate features such as hard-disk-drive controllers.

QUICKLOGIC
• WWW.QUICKLOGIC.COM

QuickLogic did not provide an update to this year's directory. The QuickMIPS family combines an embedded-processor subsystem and programmable logic on a single die. QuickLogic develops intellectual property and software to target applications that distribute digital media over Internet Protocol networks, including in-car infotainment, digital signage, overhead projectors, and medical imaging. QuickLogic offers video-compression and -decompression, encryption, and digital-rights-management modules.

RABBIT SEMICONDUCTOR
• WWW.RABBIT.COM

Rabbit Semiconductor, a Digi International company, provides high-performance, 8-bit microprocessors and development tools for embedded control, communications, and Ethernet connectivity. A sister division of single-board-computer and software manufacturer Z-World (www.zworld.com), Rabbit Semiconductor introduced the Rabbit 2000 microprocessor in 1999, the Rabbit 3000 in 2002, and the Rabbit 4000 in 2006. The company introduced the RabbitCore line of microprocessor-core modules in 2001.

NEW RAMTRON
• WWW.RAMTRON.COM

Ramtron's new Versa 8051 microcontrollers, the VRS51L2070 and 3074, target upgraded 8-bit-system applications without porting legacy code. Boasting a 40-MIPS, single-cycle, 8051 core; digital-signal-processing extensions; 64 kbytes of in-system- or in-application-programmable flash; 4 kbytes of SRAM; a JTAG-programming and debugging interface; and a robust digital-peripheral set, these devices target the performance of a 16-bit microcontroller without the need to migrate from an 8-bit device. The VRS51L3074 combines a high-perform-

Intersil Handheld Products

High Performance Analog

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- ISL8499

Battery Authentication
- ISL6296

Battery Management
- ISL6294
- ISL6299

Composite Video
- ISL59110
- ISL59111

Core Power
- ISL6273
- ISL6274
- ISL9000
- ISL9200

Fuel Gauge
- ISL6295

Light Sensor
- EL7900
- ISL29000

Voltage Reference
- ISL60007

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ance SOC (system on chip) with 8 kbytes of nonvolatile FRAM (ferroelectric RAM) to target embedded data-acquisition, sensor, and control systems.

Ramtron's Versa Mix 8051 family of integrated, high-performance, 8-bit, mixed-signal controllers targets data-acquisition, signal-conditioning, processing, and control applications. Features include a single-cycle 8051 core; a hardware MAC (multiply/accumulate) unit; an ADC; an operational amplifier; a current source; digital potentiometers; and a complete set of communication interfaces, including an I²C, an SPI (serial-peripheral interface), and UARTs.

RENESAS TECHNOLOGY
• WWW.RENESAS.COM

Renesas Technology offers a portfolio of microcontrollers and microprocessors for embedded-system applications, extending from low-power, 8- and 16-bit microcontrollers to high-performance, 32-bit microprocessors. More than 150 microcontroller offerings span operating speeds from 1 to 160 MHz and on-chip flash memories from 4 kbytes to 1 Mbyte. Renesas offers low-power, cost-sensitive, 8- to 16-bit microcontrollers in the R8C/Tiny, H8/Tiny, H8/SLP, and 740 series for home appliances, such as white goods. Renesas offers the SuperH and M16C/M32R microcontroller families for automotive, in-car-navigation, and industrial applications. The 16- and 32-bit devices in the H8 family balance function and performance for PC and server applications. The microcontrollers in the M16C and M32 families provide superior noise performance due to their excellent EMI/EMS characteristics for consumer and automotive applications. The chips in the AE series comprise a smart-card platform with 68 kbytes of EEPROM and a 1024-bit encryption coprocessor that can safeguard data and transactions for products requiring high security. The microprocessors in the SuperH families deliver high performance and on-chip peripherals for applications that use external memory. Renesas also offers SOC (system-on-chip) and SIP (system-in-package) devices, as well as analog- and mixed-signal devices for a diverse mix of applications.

The company has added 36 microcontrollers in the low-pin-count, small-package R8C/Tiny series. These devices target home appliances with low-voltage and wide-temperature-range models; 20 have LIN (local-interconnect-network) capability. The 32-bit, 40-MHz H8SX/1544F microcontroller targets instrument clusters and other automotive applications. The 266-MHz SH7763 microprocessor incorporates a floating-point unit and has two-channel gigabit-Ethernet and PCI-bus controllers. The SH7785 device for car-infotainment systems has a 600-MHz, superscalar SH-4A CPU core and provides an LCD-panel controller for displaying 2- and 3-D graphics on multiple overlapping display screens. The Euclid SH7397 targets cost-sensitive telematics systems. Renesas has added the 160-MHz SH7721 microcontroller for industrial equipment.

SAMSUNG ELECTRONICS
• WWW.SAMSUNGSEMI.COM

Samsung did not provide an update to this year's directory. The company's S3C2410 and S3C2440 minimize system cost and eliminate the need to configure additional components by featuring common peripherals for mobile applications, such as wireless handheld devices, smart phones, and GPS (global-positioning-system)-enabled portables. These processors feature a 16/32-bit

ARM920T RISC core. Both processors include a NAND-flash boot loader, and they support WinCE, Palm, Symbian, and Linux operating systems.

NEW

SEMTECH
• WWW.SEMTECH.COM

Semtech acquired Xemics and offers that company's 8- to 22-bit microcontrollers, which interface to sensors and radio transceivers and target autonomous battery-operated wireless devices. These devices operate at a constant one instruction per clock that is independent of the type of operation and addressing mode. The dedicated interface blocks, high-resolution preamplified ADC, and transceiver serializer/deserializer all enable miniature-system-wireless-sensing applications, reducing the bill-of-materials cost by eliminating external components.

The Radio Machine device for ISM (industrial/scientific/medical)-band transceiver interfacing includes a low-power RISC core with the BitJockey, a serial interface for radio protocols, and a UART. The Sensing Machine device for sensor interfacing includes a low-power RISC core with the ZoomingADC, a high-resolution sigma-delta ADC, and a programmable preamplifier. The ZoomingADC can interface to most sensors—even those with millivolt signals—without external components, reducing the cost and size of an implementation.

SHARP MICROELECTRONICS
• WWW.SHARPSMA.COM

Sharp's ARM-based, 16- and 32-bit BlueStreak microcontrollers range from ARM7 devices for cost-conscious applications to high-performance ARM9 devices for media-rich products. The 16- and 32-bit LH754xx ARM7 BlueStreak microcontrollers feature on-chip SRAM, a color and gray-scale LCD controller, CAN (controller-area-network) 2.0B, and a low-voltage detector that enables them to target applications such as GPSs (global positioning systems), PDAs, printers, copiers, security-control panels, and smart appliances. The 32-bit series of BlueStreak microcontrollers feature cache, a memory-management unit, a color-LCD controller, SRAM, a DMA controller, infrared support, pulse-width modulators, and an on-chip PLL. The ARM9 LH7A400 and LH7A404 add USB and MMC (multimedia-card) interfaces to target handheld devices such as GPSs, games, PDAs, pocket PCs, and media players.

Over the previous year, Sharp released two new ARM720T microcontrollers targeting the smart-appliance, industrial-control, and smart-toy markets.

SILICON LABORATORIES
• WWW.SILABS.COM

Silicon Laboratories' 8-bit, mixed-signal microcontrollers integrate configurable high-performance analog; a high-speed, pipelined, 100-MIPS 8051 core; in-system-programmable flash memory; and on-chip JTAG-based debugging, eliminating the need for an emulator. The company also offers a ToolStick evaluation platform, a fully contained evaluation system in a USB stick that demonstrates Silicon Laboratories' development tools.

Silicon Laboratories' precision mixed-signal, CAN (controller-area-network), small-form-factor, Ethernet, USB microcontrollers target industrial, consumer, automotive, motor-control, medical, and communications applications. The family combines high-precision analog data converters having 10 to 24 bits of resolution with a high-throughput

Microprocessor Directory

8051 CPU, making the family members ideal for analog and computationally intensive applications. The single-chip CAN-bus products integrate a CAN 2.0B controller and high-performance ADCs.

New products include the small-form-factor C8051F41x microcontrollers with 32 kbytes of flash memory and high-performance analog peripherals in a 5×5-mm package. The single-chip CP220x Ethernet controller contains an integrated IEEE 802.3-compliant MAC (media-access controller), a 10BaseT PHY (physical) layer, and 8 kbytes of nonvolatile flash memory. Silicon Labs also introduced a family of single-chip USB microcontrollers that includes an onboard USB 2.0 function controller, a transceiver, and on-chip clock recovery.

SILICON STORAGE TECHNOLOGY • WWW.SST.COM

Silicon Storage's SST65P542R, a member of an 8-bit application-specific microcontroller family, targets infrared remote controllers in the consumer segment. The SST65P542R microcontroller offers flexibility to store remote-control configurations for multiple appliances. This device integrates the multiple functions of a remote-controller system in a single-chip product.

The 89 series of 8-bit FlashFlex51 microcontrollers employ the proprietary, patented SuperFlash CMOS-semiconductor-process technology. FlashFlex51 microcontrollers target digital consumer, communication/wired, video, audio, industrial, and motor-control applications, including HDMI (high-definition-multimedia-interface) products, TVs and HDTVs, POS (point-of-sale) equipment, audio/video amplifiers, networking equipment, and home appliances.

STMICROELECTRONICS • WWW.STM.COM

STMicroelectronics offers 8-, 16-, and 32-bit microcontrollers, including ARM7- and ARM9-based microcontrollers, and application-specific devices for motor-control, USB, and CAN (controller-area-network) applications. The 8-bit portfolio includes the "bullet-proof" ST6 family, the 8051-based µPSD family, and the ST7 family. Other devices include the ST7MC for controlling three-phase brushless motors and a 3V version of the ST72324 general-purpose microcontroller. New devices include the 8-bit ST7 UltraLite, a turbo-plus version of the µPSD in a DFN package.

The company offers the 16-bit ST10 family, which includes devices operating as fast as 50 MHz with a four-stage pipeline. The 32-bit STR ARM families, based on the ARM7 and ARM9 cores, support the Thumb 16-bit ISA (instruction-set architecture) and feature peripherals such as Ethernet, USB, and CAN.

STRETCH • WWW.STRETCHINC.COM

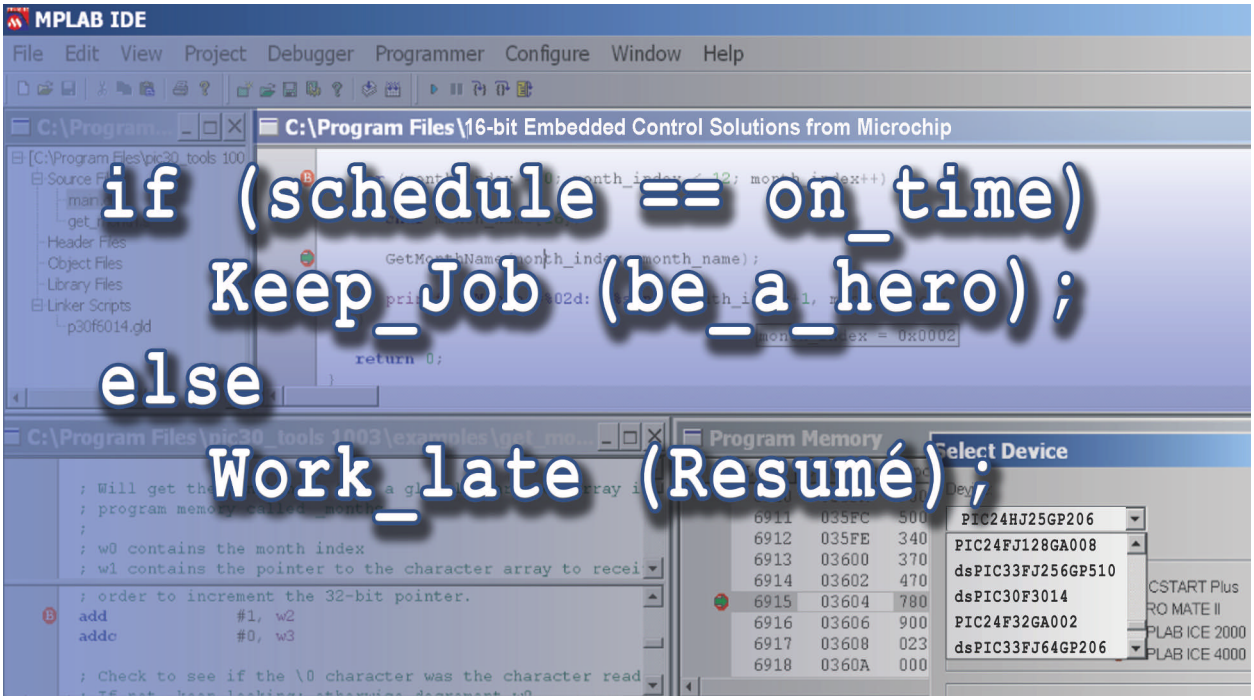
Stretch based the S5000 family of software-configurable processors on the S5 engine to boost system performance by enabling customized acceleration through the programmable logic in the processor engine. The design architecture and methodology merge the software model of general-purpose processors and the parallelism and flexibility of programmable logic to deliver customizable acceleration. The S5 engine integrates the Stretch ISEF (instruction-set-extension fabric) with Tensilica's Xtensa RISC-processor core. With Stretch's proprietary technology, developers use C and C++ to program the processor and configure the ISEF with custom instructions. The S5000 devices target computationally intensive applications, such as video and imaging and the wireless infrastructure.

TENSILICA • WWW.TENSILICA.COM

Tensilica's configurable, extensible, and synthesizable 32-bit Xtensa processor cores mold to your application by selecting and configuring predefined elements of the architecture and by inventing new instructions and hardware-execution units for maximum performance. The Xtensa processor generator automatically matches all associated software with any changes you make to the processor.

The Diamond Standard line of six processors ranges from a small, energy-efficient controller to an audio processor and a fast, high-end processor. Tensilica based the Diamond Standard family on the Xtensa configurable-processor architecture, and most members feature direct-interface ports and queues for high-speed I/O. The ultra-low-power, cacheless Diamond 108Mini RISC controller has 15 interrupts and three built-in timers. The midrange Diamond 212GP RISC controller has instruction and data caches and user-defined local-memory sizes. The midrange Diamond 232L CPU has a memory-management unit for Linux OS support. The low-power, 24-bit Diamond 330HiFi audio processor targets audio and speech codecs. The company also offers the three-issue-VLIW (very-long-instruction-word), eight-way-SIMD (single-instruction-multiple-data) Diamond 545CK

Stay on Schedule



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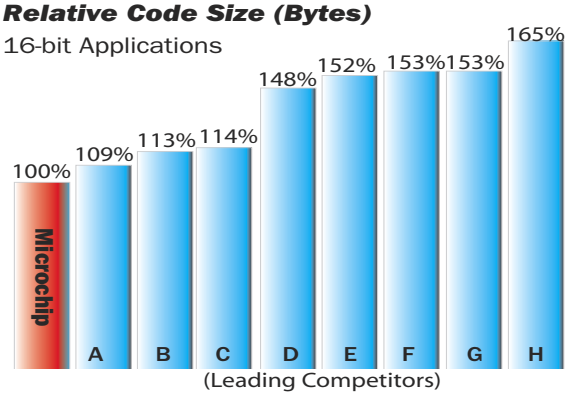

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Microprocessor Directory

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TEXAS INSTRUMENTS
• WWW.TI.COM

TI has announced plans to add more than 50 devices within two years to the 16-bit, ultralow-power MSP430 RISC-microcontroller platform. The expansion kicked off with the 14-pin, 4×4-mm MSP430F20xx microcontroller series, offering 16-MIPS processing power, a self-wake-up mode that uses less than 1 µA of power, and a 500-nA standby mode that the device achieves through VLO (very-low-power-oscillator) technology. These tiny, low-pin-count devices target space-constrained, battery-powered consumer, security, and sensing applications for which OEMs may reduce cost and liability with factory-installed, sealed batteries that last more than 10 years. MSP430F20xx devices also act as tiny system-power supervisors for larger system processors in imaging, video, and audio applications, such as digital cameras, set-top boxes, and MP3 players.

Continuing the portfolio expansion, TI introduced the MSP43FG461x microcontroller series, the first to incorporate the new MSP430X architecture. It offers a 1-Mbyte memory compared with the currently available 64-kbyte memory. The FG461x SCOC (signal-chain-on-chip) series targets portable medical devices, such as glucose meters, digital pulse oximeters, and wireless electrocardiograms that require highly integrated intelligent peripherals and larger memory options on a single chip.

TI has also announced the eZ430-F2013 microcontroller-development tool, which developers use to evaluate the MSP430 microcontroller architecture and complete an entire MSP430F20xx project from start to finish. The $20 tool comes in a compact USB-stick form factor.

The TMS470 platform of ARM7TDMI-based general-purpose processors includes the MS470R1B1M microcontrollers, now available in volume quantities.

TOSHIBA AMERICA ELECTRONIC COMPONENTS
• CHIPS.TOSHIBA.COM

Toshiba offers highly integrated 8-, 16-, and 32-bit CISC microcontrollers and a family of 32- and 64-bit MIPS-based RISC microprocessors. Toshiba TX System RISC reference designs comprise hardware and software platforms that provide a ready-to-use bill of materials. Platforms are available for consumer applications, such as digital TV, IP (Internet Protocol) set-top boxes, and home-entertainment gateways. For the development of system-level products, Toshiba delivers ready-to-use reference boards that contain a general-purpose board, sample compilers/debuggers, a real-time operating system, and software drivers enabling development of application software and rapid product delivery. Toshiba offers access to expert technology professionals for questions and application support.

Toshiba rounds out its microcontroller-product offering with an expanded embedded-flash-microcontroller product line of 8- and 16/32-bit microcontrollers for diverse applications, including consumer and industrial. Toshiba introduced the TMP92CZ26-AXBG, a 32-bit CISC microcontroller that provides 80-MIPS computing performance with power consumption of only 80 mW and incorporates 288 kbytes of RAM; it targets a range of applications including mobile/wireless designs. Toshiba also introduced the 32-bit TMP19A64F20AXBG RISC microcontroller, which operates at 54 MHz and incorporates 2 Mbytes of Toshiba's Nano flash technology; it targets consumer battery-operated applications, including digital videocameras.

TRANSMETA
• WWW.TRANSMETA.COM

Transmeta develops and licenses computing, microprocessor, and semiconductor technologies and related IP (intellectual property). Transmeta first designed, developed, and sold x86-compatible, software-based microprocessors. The company now also provides, through strategic alliances and under contract, engineering services that leverage the company's microprocessor-design and -development capabilities. The company also licenses advanced power- management technologies for controlling leakage and increasing power efficiency in semiconductor and computing devices.

Transmeta's x86-compatible Efficeon microprocessor features a 256-bit-wide VLIW (very-long-instruction-word) engine that executes as many as eight instructions per clock cycle; a 1-Mbyte L2 cache; and support for MMX (multimedia-extension), SSE (streaming-single-instruction-multiple-data-extension), SSE2, and SSE3 instructions.

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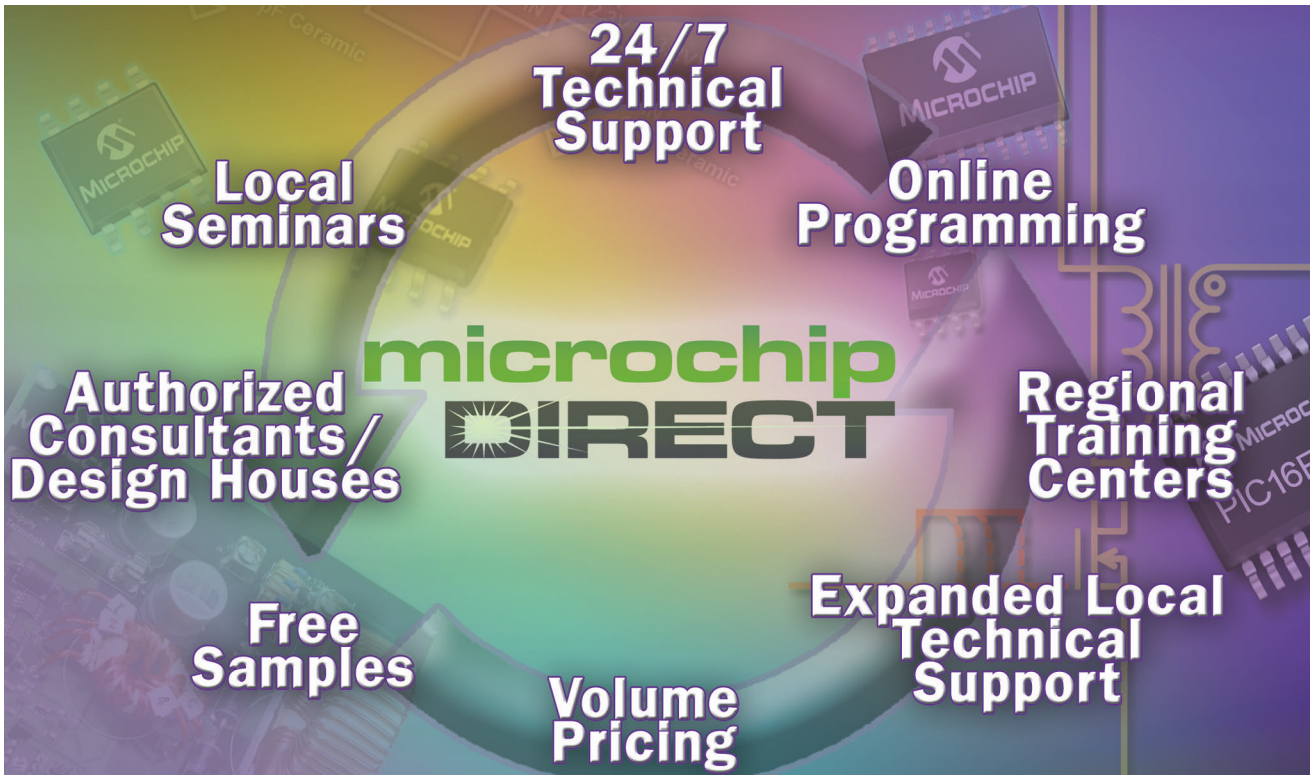

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Microcontrollers • Digital Signal Controllers • Analog • Serial EEPROMs

of real-time, interactive applications and multimedia content delivery in the digital home. The company provides optimized systems to OEMs targeting wireless routers, access points, VOIP (voice-over-Internet Protocol) gateways, streaming-media devices, print servers, and other network devices.

In 2006, Ubicom introduced the StreamEngine 5000 family of processors that build on previous product generations. Targeted at digital home infrastructure and media devices, these processors can deliver aggregate TCP/IP (Transfer Control Protocol/Internet Protocol) throughput as high as 300 Mbps to support 802.11n and wire-speed packet processing. The devices include dedicated DSP instructions for audio and high-speed interfaces such as Gigabit Ethernet and USB2.0. The SE5000 family relies on software I/O and uses a 10-way multithreaded architecture with deterministic single-cycle instruction execution.

Previous products comprise the IP2022, targeting cost-sensitive network devices, especially for 10 Base-T Ethernet and 802.11b devices, and the IP3023, which introduced zero-cycle context switching and eight-way deterministic, instruction-level hardware multithreading. The IP3023 has the performance headroom needed to drive high-performance network devices and 802.11a/b/g infrastructure equipment, including routers, bridges, and access points.

VIA TECHNOLOGIES • WWW.VIA.COM.TW OR WWW.VIATECH.COM

Via offers power-efficient processors targeting x86-based personal electronics and embedded devices with feature-rich digital-media-chip sets. Via divides its processors into five product families that it bases on power-consumption and performance criteria ranging from fanless operation to power-saving capabilities for battery-operated mobile devices. The families are the C7 and C7-M mobile, the fanless Luke, the Eden-N and fanless Eden ESP, the C3-M mobile, and the C3 processors.

XILINX • WWW.XILINX.COM

Xilinx offers processor and silicon platforms. The Virtex family of high-performance FPGAs includes the PowerPC 32-bit hard core. The configurable, general-purpose, 32-bit MicroBlaze soft core is available with Spartan and Virtex Platform FPGAs. You can supplement this core with coprocessing capabilities and a tightly integrated floating-point unit and by implementing direct connections to hardware instructions in high-performance FPGA-logic gates. For the most cost-effective applications, the 8-bit PicoBlaze microcontroller can target Spartan FPGAs and CoolRunner CPLDs.

ZILOG • WWW.ZILOG.COM

Zilog designs, develops, and markets micrologic 8-bit microcontrollers targeting both general-purpose and specific applications. Zilog offers five families of microdevices.

The eZ80 Acclaim! family provides the processing power and flash memory to implement communication-protocol stacks in applications such as communications, automation, vending machines, POS, security, industrial control, facility monitoring, and remote control. Communications peripherals include UART, I²C, SPI (serial-peripheral interface), and an IrDA (Infrared Data Association, www.irda.org) EnDec (encoder/decoder). Last year, Zilog joined the ZigBee Alliance (www.zigbee.org).

Zilog's high-performance Z8 Encore! microcontrollers include peripherals, such as ADCs and debuggers. The pure-flash Z8 Encore! XP family of microcontrollers includes a compact, eight-pin version and offers peripherals such as an ADC, a comparator, a transimpedance amplifier, a temperature sensor, and an internal precision oscillator. Last year saw the extension of the Z8 Encore! XP family with a new 12-kbyte-flash version.

Last year, Zilog launched the Z8 Encore! MC family, targeting motor-control and power-management applications. These devices feature as much as 16 kbytes of flash memory; 512 kbytes of RAM; a six-channel, 12-bit PWM; an eight-channel, 2.5-µsec, 10-bit ADC; an operational amplifier; a comparator; a 5.53-MHz internal precision oscillator; and communications protocols.

Zilog's Crimzon infrared remote-control microcontrollers, along with the company's comprehensive infrared-code database, development environments, and engineering support, offer turnkey implementations for developers developing infrared remote controllers. The infrared Crimzon ZLP12840 microcontroller integrates the ability to learn codes from other infrared remote controls through an on-chip learning circuit.

The Z8 includes the Z8 ROM, ROMless, low-voltage, and one-time-programmable families, for use mainly in low-cost, high-volume systems. In 2005, Zilog launched the Z8 GP (general-purpose) family, offering wider operating voltages; standard-, extended-, and automotive-temperature ranges; and multiple memory sizes. Zilog's legacy Z80 microprocessor architecture targets embedded-control applications. EDN

36V Input DC/DC Converters

High Performance Analog Solutions from Linear Technology

Automotive batteries, industrial power supplies, distributed supplies and wall transformers are all sources of wide-ranging high voltage inputs. The simplest method to step-down these varying sources is to use a monolithic step-down regulator that can directly accept a wide input range and deliver a well-regulated output. A group of Linear Technology's growing family of high voltage DC/DC converters accept inputs from 3.6V to 36V (or higher) and provide excellent line and load regulation and dynamic response. Nevertheless, these mid-range converters are acceptable for a wide range of applications; however, we also offer higher voltage products with inputs up to 80V. In many automotive applications, these parts are required to meet a minimum input voltage scenario, known as cold crank, where the cars battery voltage can drop to 4V, yet a regulated 3.3V is required on the output. Similarly, during a load dump scenario, transients of 36V and higher can be found at the input of the DC/DC converter which is required to regulate at a constant voltage. All of the devices offer a high efficiency solution over a wide load range with a well regulated output. The LT®3481 can deliver up to 2A of output current and offers Burst Mode® operation with quiescent current of only 50µA while the LT3493 and LT3505 can deliver up to 1.2A from a very tiny solution footprints which utilize minimal external components. See Figure 8 for a profile of our high voltage monolithic buck.

36V, 2A Step-Down Requires only 50µA Quiescent Current

The LT3481 is available in a 10-lead 3mm x 3mm DFN (or MSOP) package with an integrated 3.8A power switch and external compensation for design flexibility. The switching frequency is user programmable from 300kHz to 2.8MHz. Figure 1 shows a schematic of the LT3481 capable of producing 3.3V at 2A from an input of 4.5V to

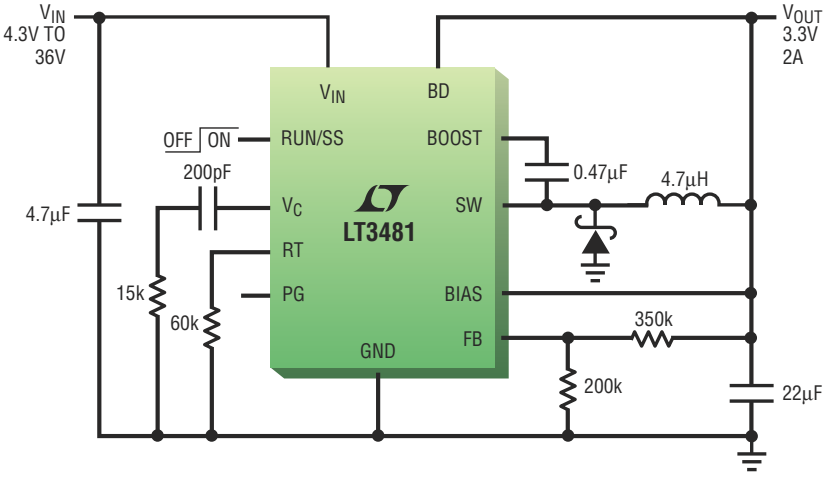

Figure 1. The LT3481 800kHz, DC/DC Converter Delivers 2A at 3.3V Output

36V Input DC/DC Converters

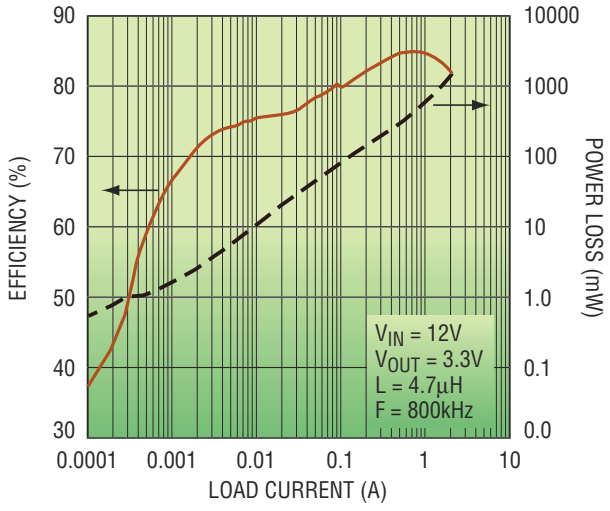

Figure 2. Efficiency vs Load Current for Figure 1 Circuit

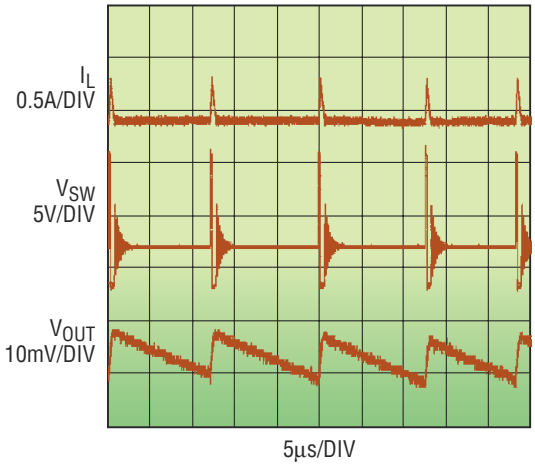

Figure 3. LT3481 Burst Mode Operation at 10mA Load Current With V_{IN}=12V For Figure 1 Circuit

36V while Figure 2 shows resultant efficiency of the circuit (with V_{IN}=12V nominal).

The LT3481 utilizes a unique low ripple Burst Mode operation which maintains high efficiency at light loads while keeping the output voltage ripple below 15mV_{PK-PK} (Figure 3). Low noise operation can be critical if there are any noise-sensitive circuits such as wireless transceivers close by. During Burst Mode operation, the LT3481 delivers single cycle bursts of current to the output capacitor followed by sleep periods when the output power is delivered to the load by the output capacitor. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current to 50µA. Figure 3 shows the inductor current and output voltage ripple under single pulse Burst Mode operation from 12V input to 3.3V output. As the load current decreases to a no load condition, the percentage of time that the LT3481 operates in sleep mode increases and the average input current is greatly reduced resulting in high efficiency. The LT3481 also has a very low shutdown current (less than 1µA) that significantly extends battery life in applications that spend long periods of time in sleep or shutdown mode.

Additionally, the LT3481's high side bootstrapping boost diode is integrated into the IC to minimize solution size and cost. When the output voltage is at least 2.8V, the anode of the boost diode can be connected to output. For output voltages lower than 2.5V, the boost diode can be tied to the input. For systems that rely on a well-regulated power source, the LT3481 provides a power good flag that signals when V_{OUT} reaches 90% of the programmed output voltage. Finally, a resistor and capacitor on the RUN/SS pin programs the LT3481's soft-start, reducing maximum inrush current during start-up.

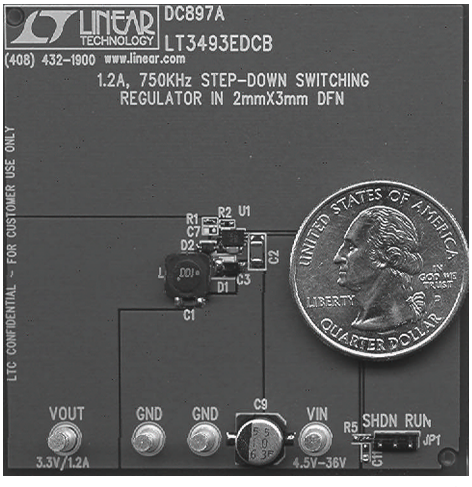

Figure 4. LT3493 Demo Board Showing <50mm² footprint

36V Step-Down DC/DC Converters Deliver 1.2A from 50mm²

Both the LT3493 and the LT3505 include an internal 1.75A, 36V power switches which are capable of withstanding 40V transients. Both parts deliver efficiencies as high as 85% from 12V inputs. Their 0.78V reference voltage enables them to operate with output voltages as low as 0.8V. Both parts offer cycle-by-cycle current limit, providing protection against shorted outputs and soft-start eliminates input current surge during start-up. The low current (<2µA) shutdown mode

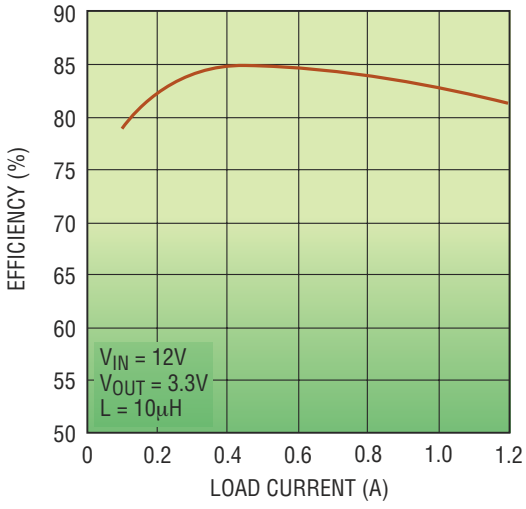

Figure 5. LT3493 Efficiency vs Output Current Curve

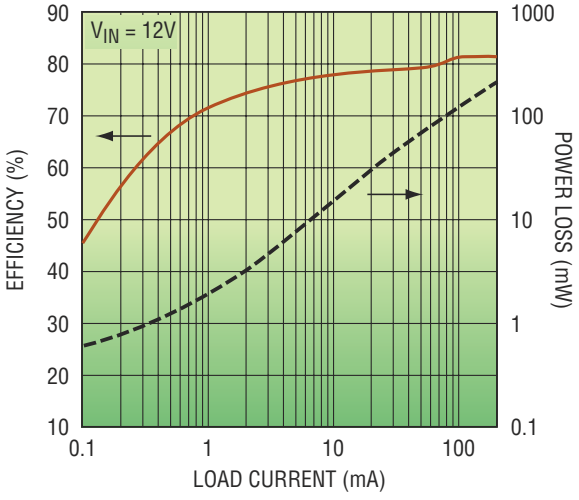

Figure 6. LT3470 Efficiency and Power Loss vs Load Current

provides output disconnect, enabling easy power management in battery-powered systems.

The LT3493 operates with a switching frequency of 750kHz in a 6-pin DFN package (2mm x 3mm). Its internal loop compensation eliminates the need for external compensation components, reducing the PC board space to less than 50mm^2. Figure 4 shows the actual size of the LT3493's solution footprint. This particular circuit generates 3.3V from a 12V input and delivers up 1.2A of output current.

The LT3505 operates with a switching frequency that is user-programmable from 250kHz to 3MHz. This enables designers to keep switching noise out of critical noise sensitive circuits while using the smallest external components possible. It is packaged in a 3mm x 3mm DFN-8 offering a very compact 36V input capable solution.

40V Step-Down Converter Deliver up to 200mA from a ThinSOT

The LT®3470 is a 40V step-down converter with the power switch, catch diode and boost diode integrated in a tiny ThinSOT™ package or 2mm x 3mm DFN. The boosted NPN power stage provides high voltage capability, high power density and high switching speed without the cost and space of external diodes.

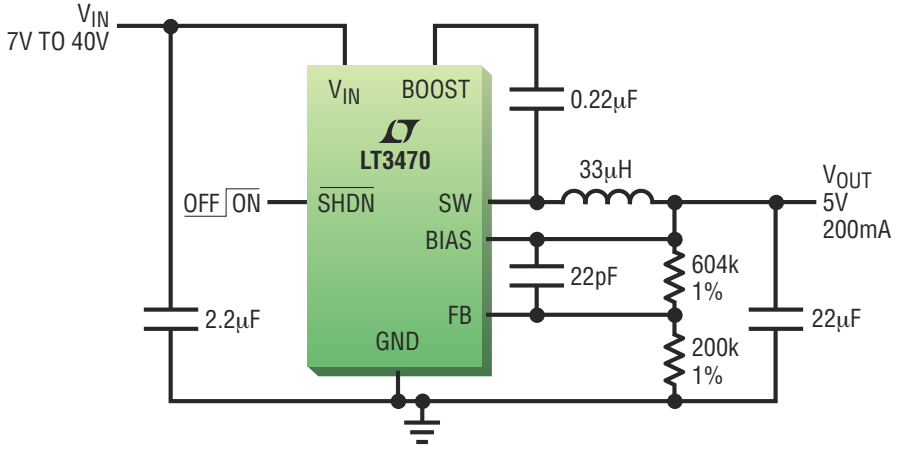

Figure 7. LT3470 Circuit for 40V Input to 5V at 200mA

36V Input DC/DC Converters

The LT3470 accepts an input voltage from 4V to 40V and delivers up to 200mA to load (Figure 7). Micropower bias current and Burst Mode operation enable it to consume merely 26µA with no load and a 12V input. Hysteretic current mode control and single-cycle bursts result in very low output ripple and stable operation with small ceramic capacitors. The combination of small circuit size, low quiescent current and 40V input makes the LT3470 ideal for automotive and industrial applications.

The LT3470 uses a hysteretic current control scheme in conjunction with Burst Mode operation to provide low output ripple and low quiescent current while using a tiny inductor and ceramic capacitors. The switch turns on until the current ramps up to the level of the top current comparator, then turns off and the inductor current ramps down through the catch diode until the bottom current comparator trips and the minimum off-time has been met. In continuous mode, the difference between the top and bottom current comparator levels is about 150mA. Since the switch only turns on when the catch diode current falls below threshold, switching frequency decreases, keeping switch current under control during start-up or short circuit conditions. If the load is light, the IC alternates between micropower and switching states to keep the output in regulation. Hysteretic mode allows the IC to provide single switch-cycle bursts for the lowest possible light load output voltage ripple (<20mV$_{PK-PK}$) from 12V to 3.3V at zero load.) During continuous switching mode at higher current levels, the output voltage ripple is even smaller (<10mV$_{PK-PK}$).

The LT3470's high level of integration, wide input voltage range and very compact solution footprint make it ideal for step down applications which require up to 40V inputs and less than 200mA of load current.

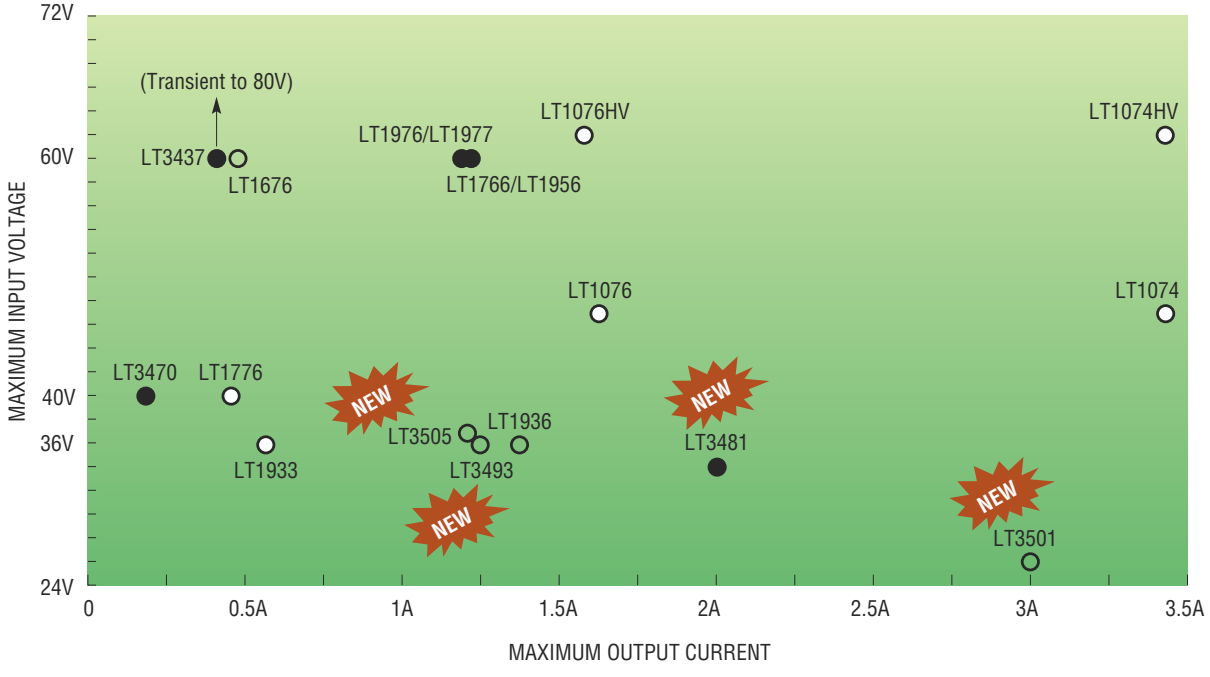

Figure 8. High Voltage Monolithic Buck Family Showing Input Voltage vs Output Current

BY JIM OLSEN AND KISHAN SHENOI • SYMMETRICOM INC

Accurate clocks optimize network service

ATOMIC CLOCKS EXTEND SIGNAL HOLDOVER TO MAINTAIN ACCURATE NETWORK TIMING AND ENSURE CONSISTENT SERVICE QUALITY DURING A GPS OUTAGE.

Wire-line- and wireless-communication systems depend on continuous access to a reliable PRS (primary-reference-source) timing signal to ensure high-quality service, especially for real-time applications, such as voice, IPTV (Internet Protocol television), and online gaming. Accurate and stable timing plays a critical role in maintaining synchronization between connected nodes in the network. Synchronized nodes improve handshaking and packet transfers and minimize latency, errors, and dropped packets; they also maximize available-bandwidth usage.

The GPS (global positioning system) is an ideal reference signal because it is readily accessible, traceable to UCT (universal coordinated time), and cost-effective for many applications. However, continuous access to GPS is not always guaranteed. When the GPS-reference signal is unavailable, network elements begin to fall out of synchronization, making it more difficult to maintain a reliable network link. As a consequence, network efficiency and reliability significantly decrease, resulting in lost packets, increased network contention, and lower overall quality of service. These problems can directly impact revenue, as they do in the cellular market, in which the competitive spotlight has shifted from comprehensive coverage to network stability. Dropped calls remain one of the key reasons users cite when changing service providers.

When you lose the GPS reference, a holdover oscillator holds the last good frequency signal until the provider restores the PRS. The quality and performance of the holdover oscillator determine the service performance of the network, as well as how long it will continue to operate efficiently once it goes into holdover mode. Compact rubidium-based atomic oscillators, for example, maintain Stratum 1 quality synchronization and timing to maintain services during extended holdover periods (**Reference 1**).

Certain characteristics of a holdover oscillator are critical when timing goes into holdover operation, and it is important to select the most effective oscillator for a particular application and network element. Diligent system design can generally minimize initial frequency-offset errors, leaving the frequency-aging rate and temperature stability as the dominant performance factors determining holdover performance.

THE TIMING HIERARCHY

It is important to understand that reliable networks must maintain a timing hierarchy to avoid degrading clock-holdover mechanisms. There are many ways in which you can create loops between, for example, the CO (central office) and smaller remote offices using the POP (Post Office Protocol), because people manage and engineer provisioning rules. It is relatively easy to create a distribution-timing loop within a network, such as Network Element A providing a reference to Network Element B, which provides a reference to Network Element C, which provides a reference signal back to Network Element A (**Figure 1**). SONET (synchronous-optical-network) and SDH (synchronous-digital-hierarchy)-ring applications are particularly prone to timing loops because the architectures themselves create a loop through which timing must be distributed.

Timing loops can unexpectedly wreak havoc on the network when the network loses the primary GPS reference. The loop

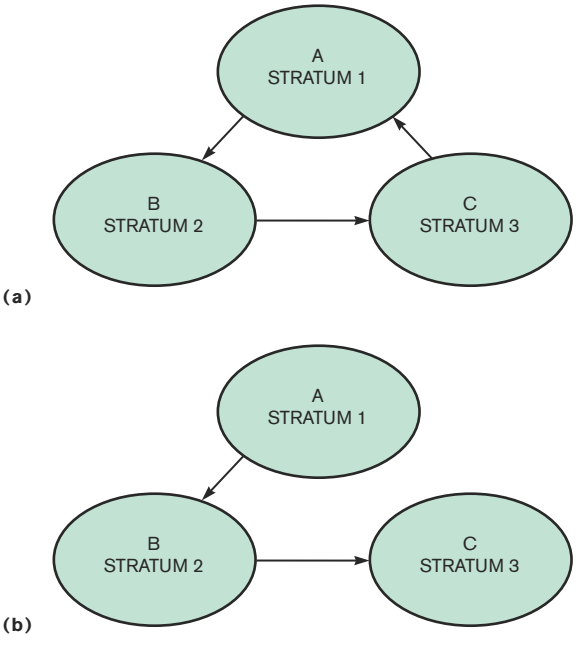

Figure 1 Distribution-timing loops (a), in which Network Element A provides a reference to Element B, which provides a reference to Element C, which provides a reference signal back to Element A, can quickly degrade holdover-oscillator timing signals unless a timing hierarchy exists (b). In a timing hierarchy, elements can receive a timing signal only from an element higher in the hierarchy.

drives oscillators to the end of their tuning range, which can create a large frequency offset that can isolate network elements and create traffic outages. The tuning range of an oscillator is a measure of how far the oscillator can move from its center frequency. The oscillator centers on the GPS-based PRS signal when it is available and maintains synchronization between network elements. When the GPS-based PRS-reference signal is unavailable, however, the oscillator pulls away from its center frequency, and the oscillators in network elements begin to pull from each other. The farther an oscillator is from its center frequency, the shorter the period of time it can provide accurate synchronization.

When a timing-reference signal passes around a loop, its accuracy quickly degrades. Consider, for example, a crystal that has a tuning range of one part in 10^8 that centers on an incoming PRS. Depending on the shared reference signal, the crystal can pull either above or below the center frequency. If the reference signal is bad or corrupted because of a timing loop, the crystal quickly pulls one way or the other to the edge of the tuning range. The narrower the tuning range of an oscillator, the less it can pull away from the center frequency. The tuning range and intrinsic accuracy of an oscillator are related entities. For example, rubidium oscillators have a tuning range (intrinsic accuracy) on the order of parts in 10^9, which means that they cannot pull far from their original PRS reference; even if you drive them to the end of their tuning range, rubidium oscillators can still maintain an accurate enough synchronization signal to avoid immediately impacting the network.

One method for distributing timing that reduces the possibility of timing loops is to propagate timing references according to a hierarchy. In other words, a timing-reference signal never follows a less accurate reference. For example, a Stratum 2 network component can feed a timing-reference signal to a Stratum 3 component, but Stratum 3 components cannot feed signals to Stratum 2 components. Thus, a signal from a less accurate holdover oscillator with a wide tuning range can never corrupt an accurate holdover oscillator with a narrow tuning range. **Table 1** shows the four stratum levels, their respective accuracy, their typical placement in a network, and the type of holdover oscillator each network requires.

It is important to be aware of the difference between a timing-reference signal that is off center frequency and one that has drifted. When a PRS is available through a GPS-based reference source, the holdover oscillator locks to the PRS because it is constantly recalibrating to the PRS. Drift comes into play when the PRS is no longer available and the system must rely on the holdover oscillator. At this point, the holdover oscillator is on its own. The accuracy of the holdover oscillator determines how quickly the center frequency of the oscillator drifts. Thus, the ability of a holdover oscillator to maintain an accurate synchronization timing reference depends on both the tuning range and the drift of the oscillator (**Figure 2**). **Table 2** compares the tuning range and drift of various oscillators.

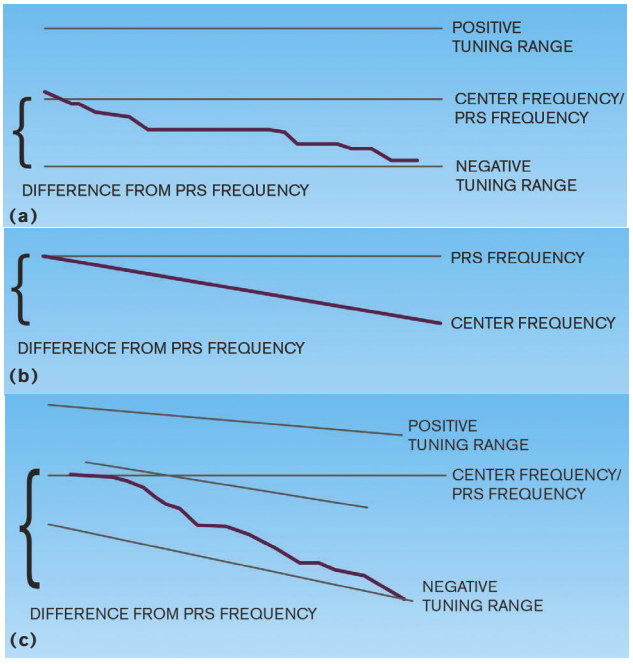

Figure 2 The tuning range of a holdover oscillator is a measure of its ability to stay close to its center frequency (a). Drift is the change in center frequency over time (b). Accurate synchronization depends on both the tuning range and the drift of an oscillator (c).

SETTLING TIME

A holdover oscillator can support a single network element or clock distribution throughout a network. This factor determines the accuracy of the oscillator's overall timing-reference signal. However, another aspect that you must consider is settling time. "Settling time" refers to how long it takes a system to adjust to the timing-reference signal from a holdover oscillator alone—that is, after it loses the PRS—as well as how long it takes a system to readjust to the PRS once the oscillator recovers the GPS-based reference signal.

Traditionally, oscillators remained on frequency through the use of a tuning voltage. As an oscillator drifted, the system would keep the oscillator on frequency by adjusting the tuning voltage. Sooner or later, however, the system would hit the end of the voltage-tuning range. Depending on the oscillator and application, this time would be two to 10 years. Now, the network element requires a manual recalibration to move the oscillator back to its center voltage.

Modern network-timing systems have eliminated the need for

(continued on page 78)

TABLE 1 STRATUM LEVELS, PRECISION, PLACEMENT IN A NETWORK, AND BEST SUITED OSCILLATOR

Level	Accuracy	Place in network	Holdover oscillator
Stratum 1	PRS: 1×10^{-11}	Synchronization feed	Local cesium clock or rubidium oscillator
Stratum 2	9×10^{-10}	Synchronization elements	Rubidium oscillator
Stratum 3	Parts in 10^{-8}	Network elements (typically end office)	Ovenized crystal oscillator
Stratum 4	Parts in 10^{-6}	Network elements (typically customer premises)	Crystal oscillator

LINEAR TECHNOLOGY

DESIGN NOTES

Pass HDMI Compliance Tests with Ease – Design Note 394

Bill Martin

Introduction

The high definition multimedia interface (HDMI) is fast becoming the de facto standard for passing digital audio and video data in home entertainment systems. This standard includes an I²C type bus called a display data channel (DDC) that is used to pass extended digital interface data (EDID) from the sink device (such as a digital TV) to the source device (such as a digital A/V receiver). EDID includes vital information on the digital data formats that the sink device can accept. The HDMI specification requires that devices have less than 50pF of input capacitance on their DDC bus lines, which can be very difficult to meet. The LTC®4300A's capacitance buffering feature allows devices to pass the HDMI DDC input capacitance compliance test with ease.

LTC4300A-1 Bus Buffer

The LTC4300A-1 is a 2-wire bus buffer that includes capacitance buffering between input and output, an enable pin for input-to-output connection control through hardware and rise time accelerators to provide for swift bus transitions through the bus logic thresholds. Due to the sub-10pF input capacitance of the LTC4300A-1, the capacitance buffering right at the HDMI connector interface allows the component to easily pass the DDC input capacitance test limit of 50pF even if the internal capacitance of the channel is substantially higher. The HDMI cable connector must see the OUT side of the LTC4300A-1 for the input capacitance compliance testing to be accurate.

In HDMI, the sink pulls the hot plug detect (HPD) signal high to tell the source that it is ready to accept commands through the DDC. This signal can be controlled by the READY pin of the LTC4300A-1 to prevent the possibility of erroneous attempts by the source to contact the sink before the sink is ready to return EDID. The READY pin only goes high after 5V is applied and the LTC4300A-1 ENABLE pin is pulled high by the HDMI receiver IC, a controller in the sink, or the 5V line itself.

The rise time accelerators in the LTC4300A-1 compress transition times on rising signal edges, minimizing the chance of interrupted data transfer due to noise and allowing the DDC to meet I²C timing requirements. That is, HDMI specification allows for 800pF of load; enough that the DDC cannot be guaranteed to meet the required 100kHz I²C 1µs rise time specification with the allowed DDC pullup resistance values. Rise time accelerators allow this timing requirement to be met even with capacitances well above 800pF.

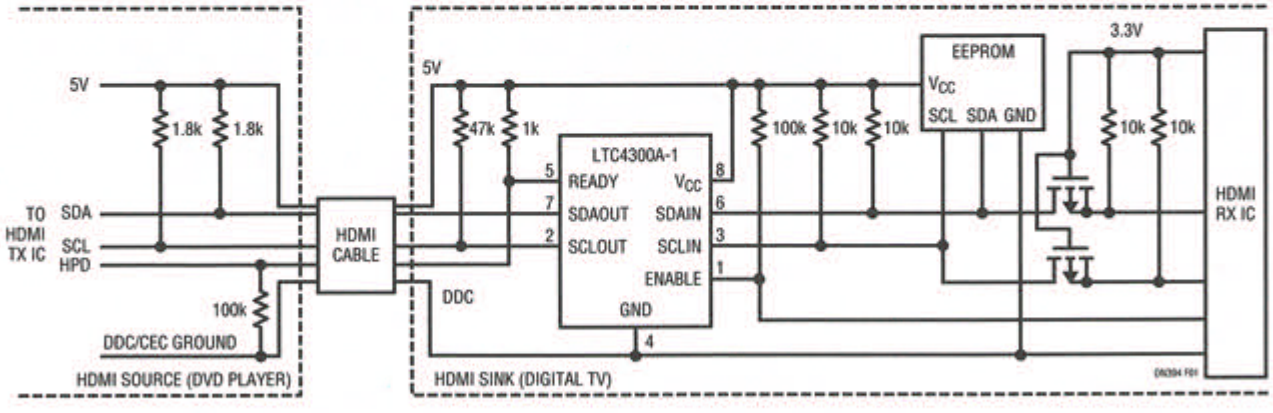

Figure 1. LTC4300A-1 in HDMI Capacitance Buffering Application

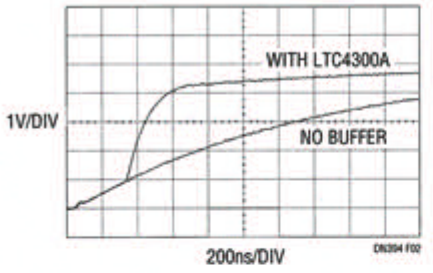

Figure 2. The LTC4300A Provides Capacitance Buffering for the DDC while Improving Bus Timing

If the 5V supply for the DDC is changed to 3.3V in future versions of the HDMI specification, the LTC4300A-1 can remain in the design as is, for it can work with supply voltages from 2.7V to 5.5V. The LTC4300A-1 will transparently support new and legacy equipment in the case of an HDMI specification change.

Figure 2 shows how the LTC4300A-1 provides capacitance buffering at the cable interface while improving the rise time of the heavily loaded 5V bus (750pF in this example). Without the LTC4300A-1, the signal is failing the I^2C 1µs rise time specification (measured between $0.3V_{CC}$ and $0.7V_{CC}$). In the DDC capacitance test, only the capacitance of the connector, the traces to the LTC4300A-1 and the less than 10pF input capacitance of the LTC4300A-1 will be measured.

LTC4300A-3 Level Shifting Buffer

The LTC4300A-3 level shifting I^2C buffer is also a good solution for this application. Figure 3 shows the LTC4300A-3 being used for capacitance buffering and 5V to 3.3V level shifting. In this application, the EEPROM is powered by a backup 3.3V supply that is available when the component is turned off. The EDID in the EEPROM should be available for reading even when a component's power is off. The level shifting between the 5V and 3.3V bus segments is accomplished by having separate supply pins for the two segments.

Having two supply pins also allows the LTC4300A-3 to provide rising edge acceleration on the 3.3V and 5V bus segments. This is a useful feature for the bus segment that is inside the component, but cable capacitance values of well over the 700pF HDMI spec will be encountered in the up to 30m HDMI cables that are being used for home theaters, so rise time acceleration is a most valuable feature on the cable side bus segment.

Although the applications shown are for HDMI receive channels, the LTC4300A-1 and LTC4300A-3 can also be used in HDMI transmit channels with equal success.

Conclusion

The LTC4300A-1 and LTC4300A-3 solve the DDC capacitance testing problem in HDMI while also substantially improving the timing performance of the bus and providing a high level of ESD protection.

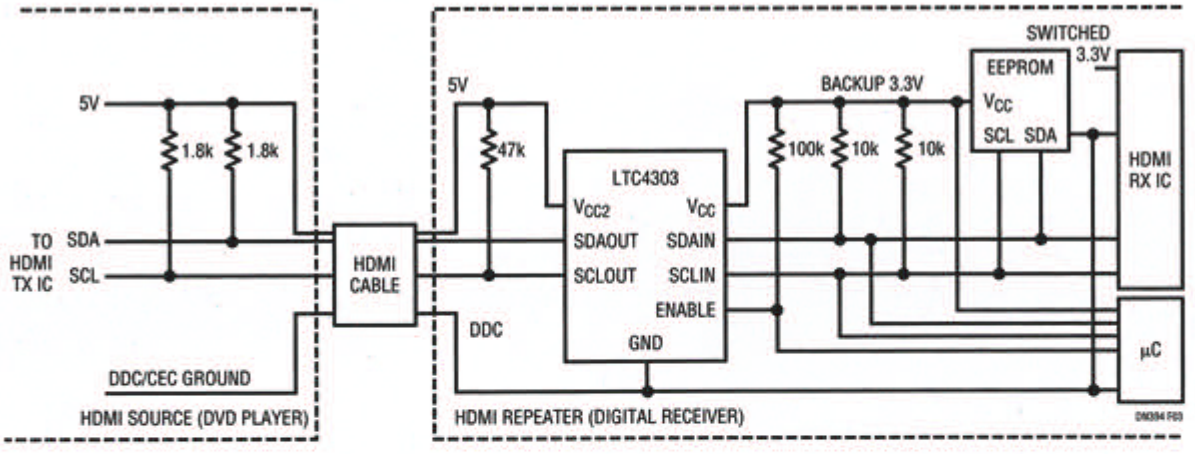

Figure 3. LTC4300A-3 in a Level Shifting and Capacitance Buffering HDMI Application with Backup 3.3V

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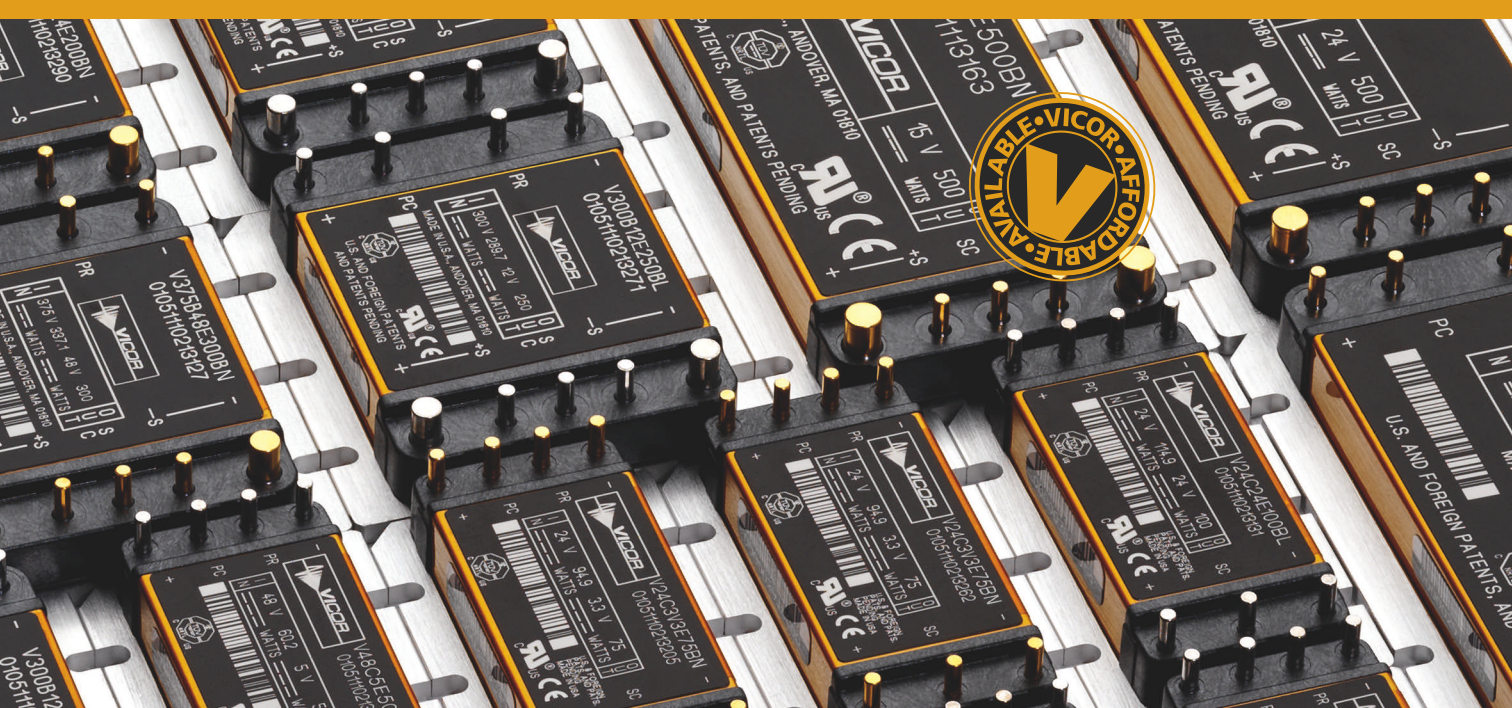

TABLE 2 OSCILLATOR TYPES, ACCURACY, AND DRIFT

Technology	Intrinsic accuracy	Stability (1 sec)	Stability (floor)	Initial to ultimate aging (per day)	Hold Stratum 1	Cost
Hydrogen maser	$\sim10^{-10}$	$\sim10^{-13}$	$\sim10^{-15}$	10^{-15} to 10^{-16}	Years	~200×
Cesium beam	$\sim10^{-11}$	$\sim10^{-11}$	$\sim10^{-14}$	NA	NA	~20×
Rubidium-gas cell	$\sim10^{-9}$	$\sim10^{-11}$	$\sim10^{-13}$	10^{-11} to 10^{-13}	Days	~×
High-quality quartz	10^{-6} to 10^{-8}	$\sim10^{-12}$	$\sim10^{-12}$	10^{-9} to 10^{-11}	Hours	~0.7×

and high expense of manual tuning through the use of DDS (direct digital synthesis). DDS circuitry allows the use of a free-running oscillator to create an internal reference signal that can lock to the incoming PRS feed. DDS circuits use well-known digital elements, such as accumulators. A digital word controls the output-frequency rate, simplifying microprocessor control. The precision of the system can generate a frequency value that directly links to the word length of the implementation. The range of a DDS circuit is so large that it can easily compensate for the drift in an oscillator over more than 20 years.

When the system loses the GPS-based PRS feed, DDS relies solely on the signal from the oscillator, which differs somewhat from the combined PRS-plus-oscillator reference. If the change in reference frequency is too large, it causes a phase transient in the timing signal that may cause network elements to unlock. As these elements attempt to relock to the reference signal, the network element will experience disruptions, errors, and dropped traffic. To avoid losing lock, the system must adjust slowly over time to the new reference signal.

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Settling occurs whenever the reference-timing signal of a network element changes. Thus, even if the system only briefly loses the GPS-based reference signal, the system needs to settle to adjust to both the loss and the immediate regaining of the PRS. The longer the settling time, the greater the impact on system reliability.

In general, settling time depends on the overall difference between the PRS and the holdover frequency. The farther the frequency has drifted, the longer the settling time. Tuning range also comes into play, because the narrower the tuning range, the faster an oscillator can settle and restore network stability.

PUTTING IT ALL TOGETHER

As you can see, you must consider many variables when selecting a holdover oscillator to use at each level of a network. Typically, the more accurate and reliable an oscillator is, the more expensive it is. Arbitrarily using less accurate holdover oscillators directly affects network reliability. On the other hand, specifying too accurate a holdover oscillator unnecessarily increases system cost.

First, consider how long a system can afford to operate using a holdover frequency. If a technician can quickly address the loss of a PRS, then no pressing need exists for a long-term holdover capability. However, if signal loss could extend across days or weeks, more accurate holdover is the only way to maintain the synchronization to uphold network reliability during this time. A second relevant aspect to consider is accuracy. Crystal oscillators provide a sufficient timing signal for hours to days. Hence, after a few hours or days, timing accuracy for this network element decreases to the accuracy of the crystal rather than to the original reference or PRS that the oscillator was following. For mission-critical applications, a rubidium oscillator holds an accurate reference for more than 30 days, depending on the application.

Developers also need to consider the overall impact of a holdover oscillator on the system. For example, if a network element propagates timing signals down through the timing hierarchy, a less accurate holdover oscillator speeds the degradation of holdover oscillators further down the hierarchy. Finally, developers need to take into account the impact that settling time has on the network. For example, although a network element may require only the precision of an ovenized crystal oscillator, a developer may opt to implement a rubidium oscillator to minimize settling time and, as a result, reduce the impact of PRS loss and gain.

Synchronization is the foundation of reliable connectivity in networks. Using an accurate timing hierarchy maximizes bandwidth usage and uptime. Reliable networks require the presence of a holdover oscillator to maintain accurate network timing when something interrupts access to a PRS. By understanding the difference between oscillator precision, drift, tuning range, and settling time, engineers can select the most cost-effective and reliable holdover oscillator to reduce unnecessary system downtime and loss of service quality. EDN

REFERENCE

1 "Synchronization Interface Standards for Digital Networks," American National Standards Institute, ANSI/T1.101-1998, www.ansi.org.

AUTHORS' BIOGRAPHIES

Jim Olsen is a business-development director at Symmetricom (San Jose, CA), where he has worked since 1984. He has designed and implemented telecommunication-synchronization networks and works with telecom manufacturers on adopting and integrating new technologies. Before joining Symmetricom, he served for six years in the US Navy in electronic warfare. Olsen is a much-sought-after speaker at national and international conferences and has authored numerous white papers and articles about synchronization and next-generation networks.

Kishan Shenoi, PhD, is a chief technologist at Symmetricom (San Jose, CA), where he has worked since 1992. He works on the research and development of the company's synchronization and timing technologies from the conceptual phase to the prototype phase. The industry knows him as Professor Sync, the dean of Sync University, an online, industry-neutral forum that provides network engineers information ranging from synchronization basics to next-generation network issues. Shenoi has written numerous white papers and application briefs about issues that affect telecom-synchronization networks. He received a doctorate in electrical engineering from Stanford University (Stanford, CA).

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LTC3205	2.8 to 4.5	250	3	Main, SUB, RGB	9	SPI*	4 x 4 QFN-24
LTC3209-1/-2	2.9 to 4.5	600	3	Main, CAM, Aux	8	I²C	4 x 4 QFN-20
LTC3210/-1	2.9 to 4.5	500	2	Main, CAM	5	1-wire	3 x 3 QFN-16
LTC3217	2.9 to 4.5	600	1	CAM	4**	Resistor/PWM	3 x 3 QFN-16
LTC3214	2.9 to 4.5	500	1	CAM	1**	Resistor/PWM	3 x 3 DFN-10
LTC3216	2.9 to 4.4	1000	1	CAM	1**	Resistor/PWM	3 x 4 DFN-12

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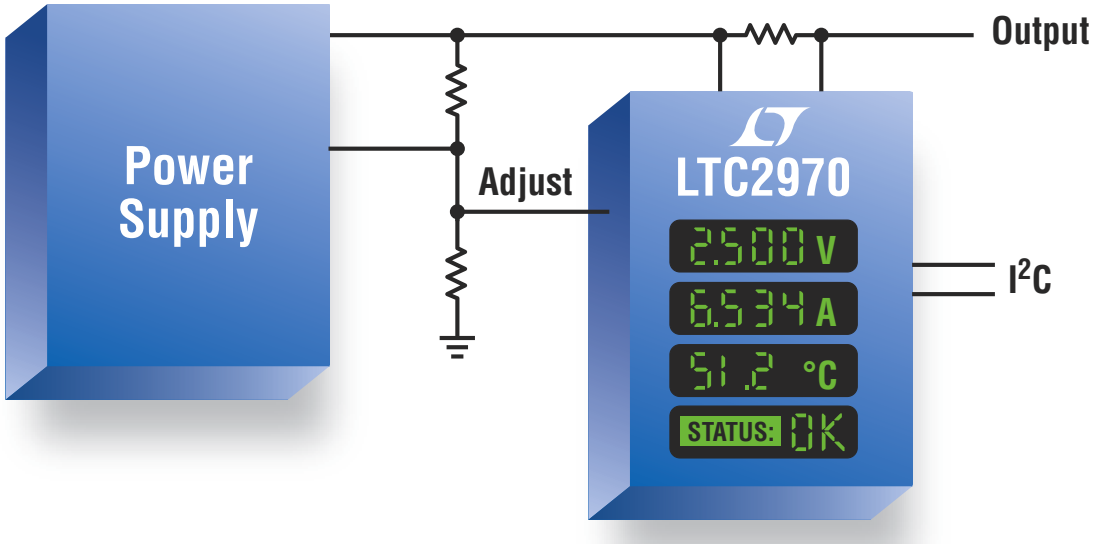

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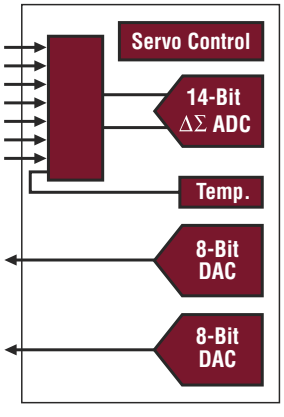

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READERS SOLVE DESIGN PROBLEMS

Low-dropout regulator, SMPS cascade suppress ripple, maintain efficiency

Scot Lester, Texas Instruments, Dallas, TX

A step-down SMPS (switched-mode power supply) efficiently converts unregulated power to a regulated output voltage. However, unwanted switching-induced ripple and input transients may appear on the output. Applying noisy power to an RF power amplifier can inject spurious signals or modulated noise into the broadcast spectrum. Analog- and RF-system engineers favor traditional low-noise power-supply designs that comprise a transformer, rectifier, and filter followed by a linear voltage regulator. A low-dropout linear regulator's low output noise and high PSRR (power-supply rejection ratio) ensure clean power that imposes no interference on a power amplifier's output.

Unfortunately, a transformer-and-rectifier power supply delivers a fluctuating output voltage that depends on its input voltage. As the difference between its input and output voltage increases, a low-dropout regulator's efficiency decreases, and its power dissipation increases. To remain in regulation at low ac-line voltages, even a low-dropout regulator requires a certain amount of head-room input-to-output voltage.

To overcome the disadvantages inherent in both circuits, you can use an SMPS to maintain high efficiency and a low-dropout regulator to reduce the output noise and ripple voltage of the SMPS. Setting the output voltage of the SMPS slightly higher than the low-dropout regulator's minimum dropout voltage reduces the regulator's power dissipation, accommodates the voltage margin you need for good switching-noise rejection, and maintains high efficiency. The regulators' PSRRs add, and the combined circuits' PSRR exceeds that of either the regulator or the SMPS alone.

Figure 1 shows a cascade circuit comprising an SMPS followed by a linear regulator. This circuit's output voltage ranges from 1.5 to 5V at an output cur-

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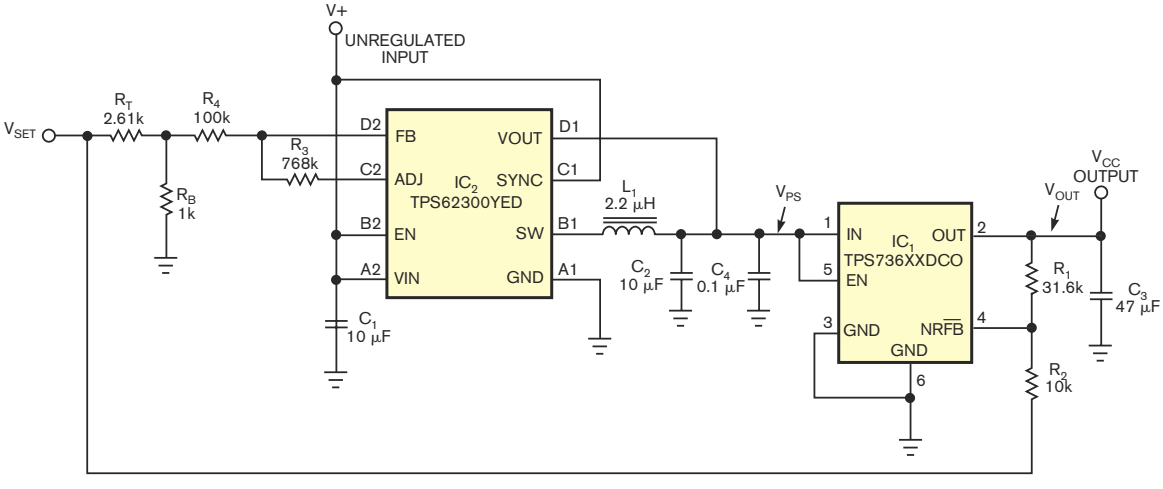

Figure 1 Connected in cascade, a low-dropout linear regulator and a switched-mode power supply improve output-voltage ripple and maintain overall efficiency. (Note: In IC_1's part designation, "XX" represents the regulator's output voltage.)

rent as high as 400 mA. Although a fixed 6V supply powers the cascaded circuit, its design accommodates any input voltage at least 0.5V higher than the cascaded pair's desired output voltage.

Adjusting the reference voltage, V_{SET}, over 0 to 1.105V linearly varies the circuit's output voltage. Resistors R_1 and R_2 and reference voltage V_{SET} determine the low-dropout regulator's output voltage and thus the cascaded pair's output voltage. Resistors R_T, R_B, R_3, and R_4 divide V_{SET} to maintain the SMPS' output voltage, V_{PS}, at a constant 0.2V higher than the regulator's output voltage, reducing the regulator's power dissipation to 80 mW at full output current and any output voltage.

At its maximum output current of 400 mA, the cascaded supply reaches a maximum efficiency of 89% with a 6V input and a 4.69V output (**Figure 2**). The overall efficiency decreases as the output voltage decreases. **Figure 3** compares the PSRRs of the SMPS alone and of the SMPS cascaded with the regulator, which improves PSRR by 46 dB at 500 Hz—essentially that of the regulator alone at 500 Hz.

Over a frequency range of 100 Hz to 100 kHz, the low-dropout regulator improves PSRR by at least 25 dB (**Figure 3**). Circuit-layout and -measurement techniques compound the difficulty of making accurate small-signal measurements, and the graph's PSRR values may not appear additive. The linear regulator governs the circuit's switched-load transient response, which may represent an improvement over the response of the SMPS. However, the cascade circuit's low output ripple and high efficiency make the circuit well worth investigation. EDN

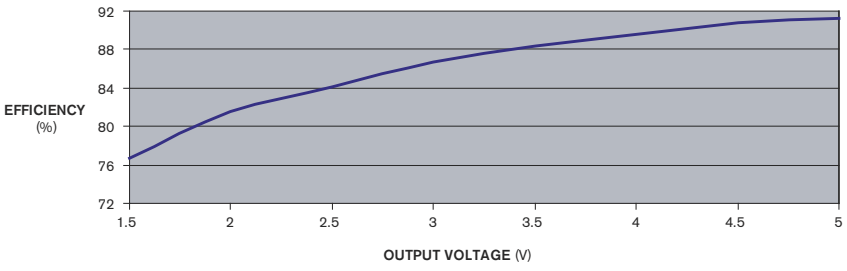

Figure 2 The regulator cascade's combined efficiency improves as the unregulated output voltage increases.

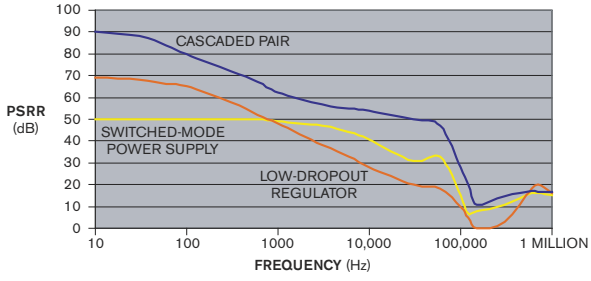

Figure 3 The power-supply rejection ratio improves significantly (blue trace) when you cascade switched-mode (yellow trace) and linear (red trace) voltage regulators.

Novel circuit isolates temperature sensor from its host

Alfredo H Saab and Tamer Mogannam,
Maxim Integrated Products Inc, Sunnyvale, CA

Temperature sensors must sometimes operate at locations whose return potentials differ considerably from that of the data-acquisition system's common—that is, equipotential—ground. In consequence, the temperature sensor's support circuitry must provide galvanic isolation between the sensor and its data-acquisition system. Also, the data-acquisition system seldom provides an isolated source of power for the sensor. The circuit in **Figure 1** solves both problems by isolating the sensor's signal and power supply.

The complementary, fixed-frequency square-wave outputs of a power-transformer driver—IC_1, a Maxim (www.maxim-ic.com) MAX845—drive a Halo Electronics (www.haloelectronics.com) TGM-010P3 1-to-1-to-1 transformer with dual primary windings and a single untapped secondary winding (**Reference 1**). The secondary winding feeds a Graetz-bridge rectifier that generates approximately 4.5V to power IC_2, a Maxim MAX6576 sensor. Combining a temperature sensor, signal-processing electronics, and an easy-to-use digital-I/O interface in a low-cost package, the MAX6576 draws little current from a single supply source and maintains its specified accuracy over a 3 to 5V supply-voltage range.

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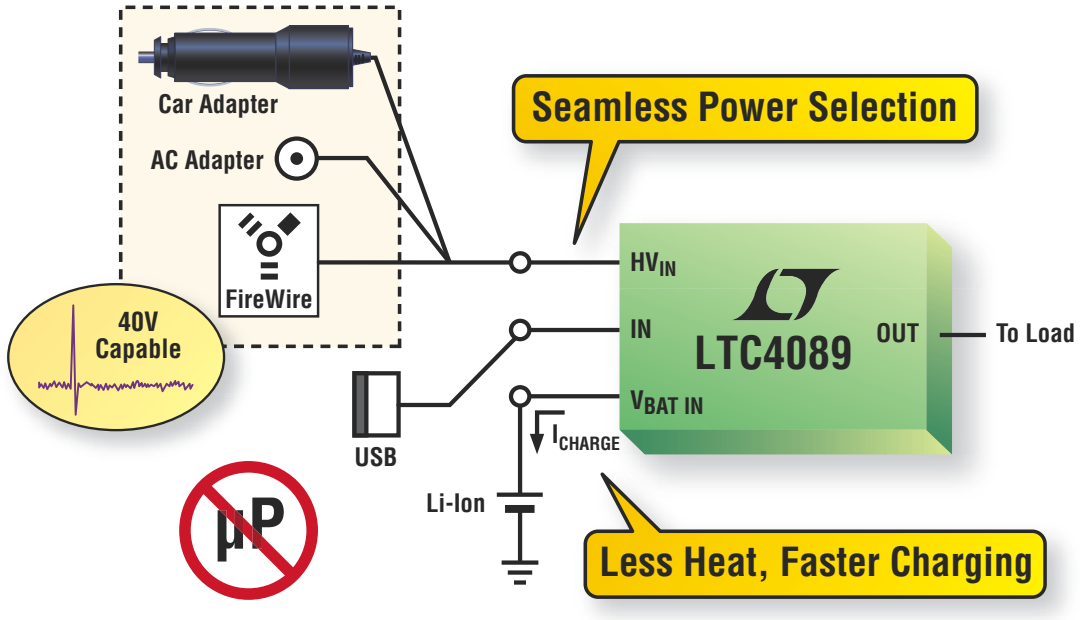

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LTC4055	1.25A	4.3V to 5.5V	Timer	4mm x 4mm QFN-16	PowerPath Control with Low Loss Ideal Diode
LTC4075	950mA or 650mA USB	4.3V to 8V	C/x	3mm x 3mm DFN-10	Dual Input: USB or Adapter
LTC4076	950mA or 650mA USB	4.3V to 8V	C/x	3mm x 3mm DFN-10	Dual Input: USB or Adapter; C or C/5 USB Charge Current
LTC4077	950mA or 650mA USB	4.3V to 8V	C/10	3mm x 3mm DFN-10	Dual Input: USB or Adapter; C or C/x USB Charge Current

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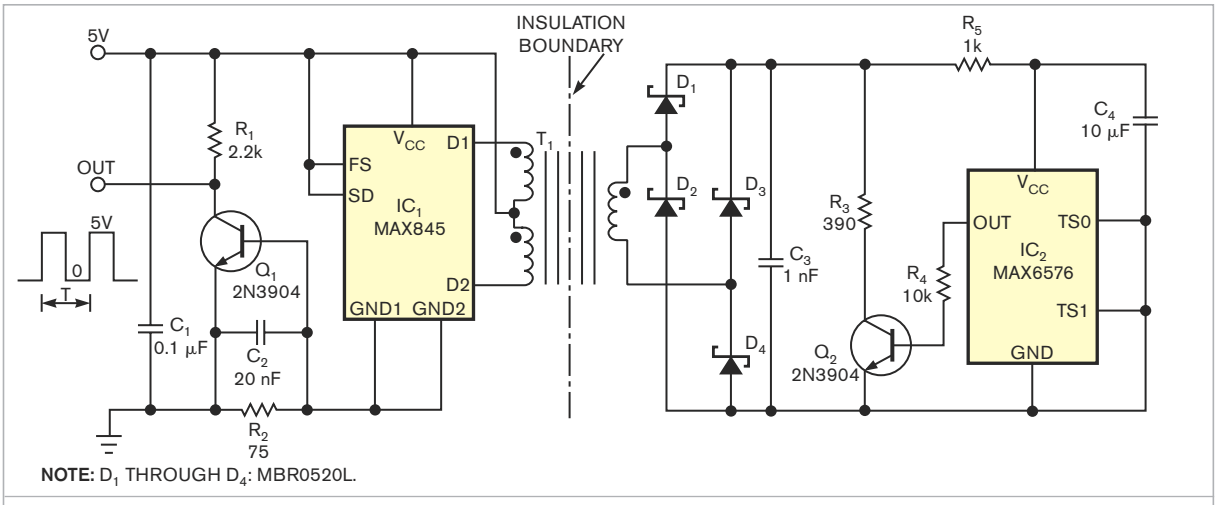

Figure 1 Transformer T_1 isolates the temperature sensor, IC_2, from the equipment under test. The period of IC_1's digital output varies as a function of temperature. The circuit's output period varies at a rate of 10 µsec/°K. User-selected scale factors range from 10 to 640 µsec/°K.

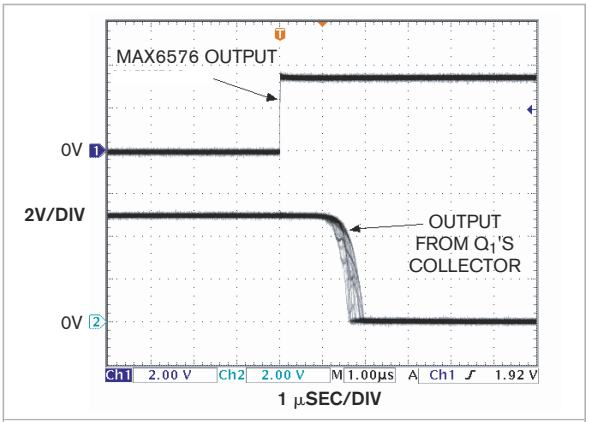

Figure 2 Measured from the positive-going edge of IC_2's output to the circuit's output at Q_1's collector, the relative jitter averages less than 1 µsec.

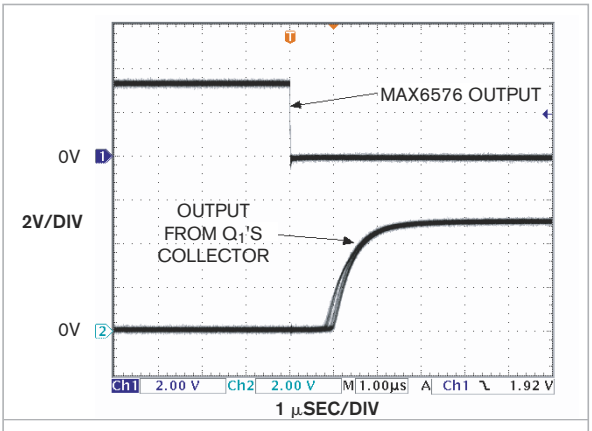

Figure 3 As in Figure 2, Q_1's average output jitter with respect to IC_1's negative-going output also averages less than 1 µsec.

If you connect the sensor as **Figure 1** shows, it operates as an absolute temperature-to-period converter and provides a nominal conversion constant of 10 µsec/°K, which, at room temperature, yields a period of approximately 2.980 msec—a frequency of 335 Hz. You can adjust the conversion constant from 10 to 640 µsec/°K. Note that longer conversion constants allow more signal-integration time to minimize noise effects. The sensor's symmetrical square-wave output drives NPN transistor Q_2's base through R_4, a 10-kΩ resistor. A 390Ω resistor, R_3, serves as Q_2's collector load and connects to the same lines that deliver power to the temperature sensor. When Q_2 conducts, it draws an asymmetrical power-supply current that exceeds the supply current during the sensor output's positive half-cycle.

In IC_1's sensor output-to-ground return on the data-acquisition system's side, resistor R_2 and capacitor C_2 shunt Q_1's base-emitter junction. The values of R_2 and C_2 ensure that the sum of IC_2's current and transformer T_1's magnetizing current cannot drive Q_1 into conduction. When Q_2 conducts, it draws about 12 mA from the isolated 4.5V power-supply line. Reflecting to the primary, Q_2's conduction current flows from the 5V supply into IC_1, out through its ground terminals, and partly through R_2. The voltage drop across R_2 exceeds Q_1's base-emitter voltage threshold and supplies sufficient base current to turn on Q_1.

Thus, when Q_2 conducts, so does Q_1, which copies IC_1's isolated square-wave output to Q_1's collector circuit. As the waveforms of **figures 2** and **3** show, Q_1's output rise and fall times, jitter, and propagation delay total about 2 µsec. The equivalent measurement error due to timing jitter amounts to less than 0.1°K at the fastest conversion constant of 10 µsec/°K. Varying the circuit's supply voltage through a range of 4.5 to 5.5V introduces an error of less than 0.1°K. The output at Q_1's collector can sink several milliamperes at a voltage excursion of 0 to 5V.

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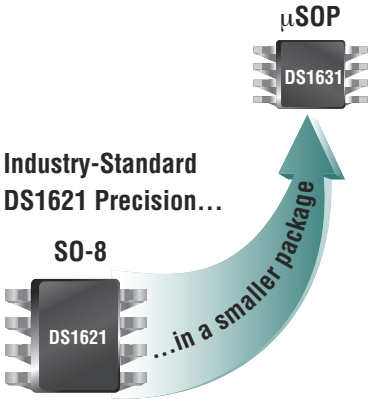

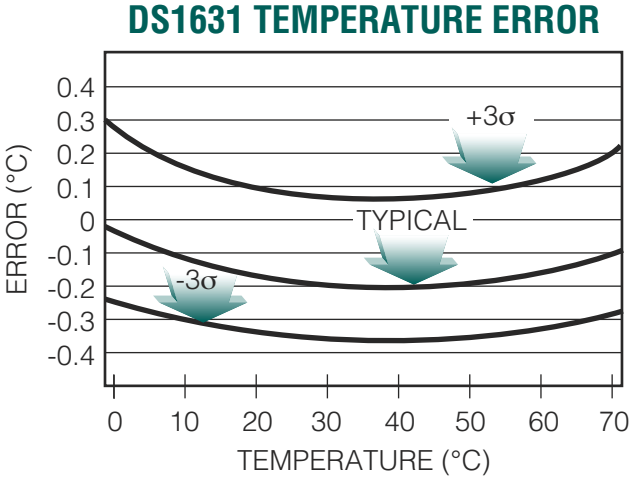

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This design can accommodate temperature-to-frequency converters and other types of temperature sensors. For further information on IC_1 and IC_2, review the devices' data sheets and the data sheet for the MAX845 evaluation kit (**references 2, 3, and 4**).EDN

REFERENCES

1 "PCMCIA DC/DC Conversion Isolation Modules," Halo Electronics Inc, www.haloelectronics.com/pdf/lowpower-oper.pdf.

2 "Isolated transformer driver for PCMCIA applications," Maxim Inc, October 1997, http://pdfserv.maxim-ic.com/en/ds/MAX845.pdf.

3 "SOT Temperature Sensors with Period/Frequency Output," Maxim Inc, April 1999, http://pdfserv.maxim-ic.com/en/ds/MAX6576-MAX6577.pdf.

4 MAX845 Evaluation Kit, Maxim Inc, October 1997, http://pdfserv.maxim-ic.com/en/ds/MAX845EVKIT.pdf.

Find resistor values for arbitrary programmable-amplifier gains

Sid Levingston, DML Engineering Inc, Aloha, OR

When available fixed-gain values match design requirements, a PGA (programmable-gain-amplifier) IC offers a drop-in choice, but what does a designer do when a suitable PGA is unavailable? Before the PGA's advent, a circuit designer who needed selectable, fixed amounts of gain chose a suitable operational amplifier and designed a switched-resistor gain-setting network. This Design Idea discusses two methods of designing the desired resistive network.

Figure 1 shows a series-ladder-resistor network comprising a string of resistors whose junctions connect to switch-selectable taps that determine the circuit's gain. Little current flows through the switch, and the resistance of the switch thus doesn't affect the design. A circuit with N discrete-gain values requires an N-position switch, usually an analog multiplexer, and N+1 resistors in its ladder. **Equation 1** describes the circuit's gain in the general case:

$$GAIN[n] = \frac{\sum_{i=1}^{n} R_i}{\sum_{i=n+1}^{N+1} R_i} + 1. \quad (1)$$

You can solve **Equation 1** for the resistor summations and expand a few terms as follows:

$$\frac{\sum_{i=1}^{n} R_i}{\sum_{i=n+1}^{N+1} R_i} = GAIN[n]-1. \quad (2)$$

$$\sum_{i=1}^{n} R_i = (GAIN[n]-1) \times \sum_{i=n+1}^{N+1} R_i. \quad (3)$$

$$R_1 = (GAIN[1]-1) \times (R_2 + R_3 + \ldots + R_{N+1}), \quad (4)$$

$$R_1 + R_2 = (GAIN[2]-1) \times (R_3 + \ldots + R_{N+1}), \quad (5)$$

and

$$R_1 + R_2 + R_3 + \ldots + R_N = (GAIN[N]-1) \times (R_{N+1}). \quad (6)$$

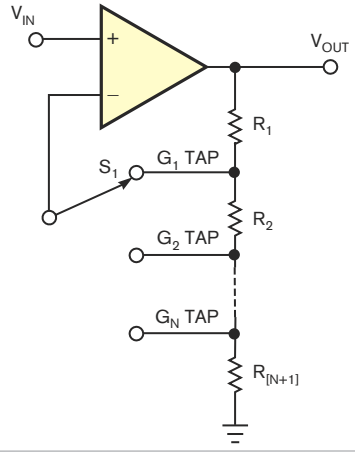

Figure 1 A series-resistor-ladder network and a single-pole, multiple-throw switch form a custom-value programmable-gain amplifier.

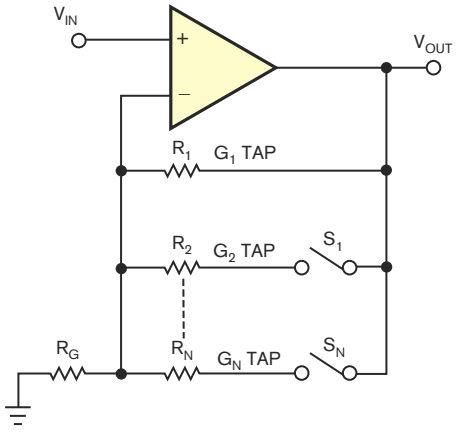

Figure 2 In a parallel-resistor-ladder network, connecting one resistor at a time in parallel with R_1 determines the circuit's gain.

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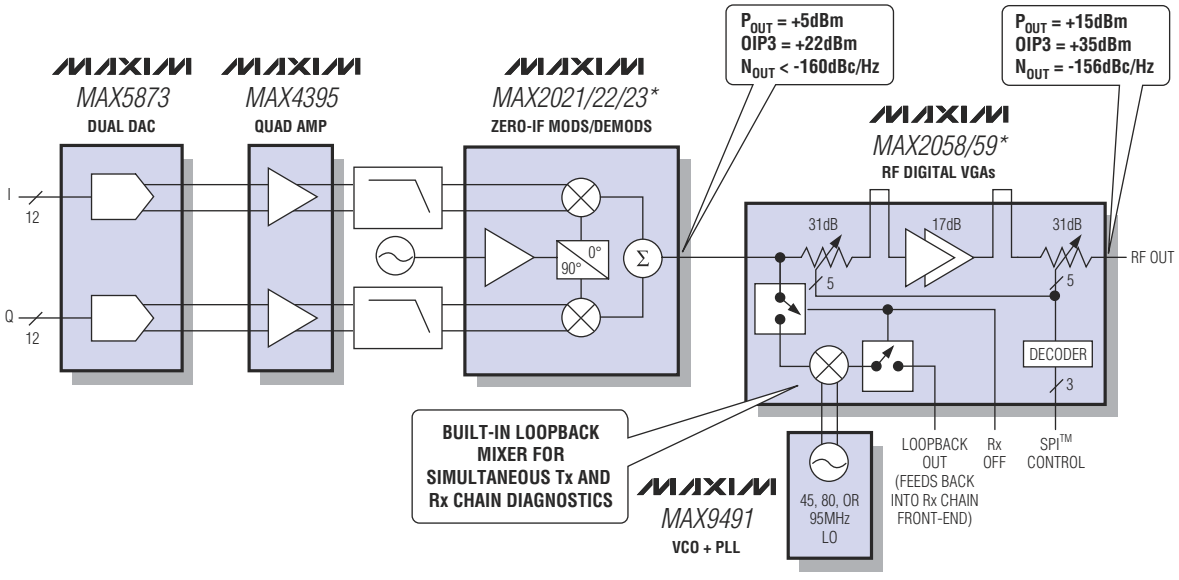

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Next, normalize R_1 to 1Ω and solve the equations for R_1:

$$1 = (GAIN[1]-1) \times (R_2 + R_3 + ... + R_{N+1}), \quad (7)$$

$$1 = -R_2 + (GAIN[2]-1) \times (R_3 + ... + R_{N+1}), \quad (8)$$

and

$$1 = -R_2 - R_3 - ... - R_N + (GAIN[N]-1) \times (... + R_{N+1}). \quad (9)$$

$$\begin{bmatrix} GAIN[1]-1 & GAIN[1]-1 & GAIN[1]-1 & GAIN[1]-1 \\ -1 & GAIN[2]-1 & GAIN[2]-1 & GAIN[2]-1 \\ ... & ... & ... & ... \\ -1 & -1 & -1 & GAIN[N]-1 \end{bmatrix} \times \begin{bmatrix} R_2 \\ R_3 \\ ... \\ R_{N+1} \end{bmatrix} = 1. \quad (10)$$

A network that synthesizes N gain values results in an N×N matrix whose upper echelon equals the desired gains minus one, in ascending order, and its lower echelon equals negative one. To produce the resistor values for the desired gains, invert the matrix and calculate its dot product with a unity matrix. For example, a circuit requiring four gain values of three, five, 24, and 50 also requires five resistors. Stuffing and solving the matrix yields:

$$\begin{bmatrix} 2 & 2 & 2 & 2 \\ -1 & 4 & 4 & 4 \\ -1 & -1 & 23 & 23 \\ -1 & -1 & -1 & 49 \end{bmatrix} \times \begin{bmatrix} R_2 \\ R_3 \\ R_4 \\ R_5 \end{bmatrix} = 1. \quad (11)$$

$$\begin{bmatrix} R_2 \\ R_3 \\ R_4 \\ R_5 \end{bmatrix} = \begin{bmatrix} 0.2000 \\ 0.2375 \\ 0.0325 \\ 0.0300 \end{bmatrix}. \quad (12)$$

Scale the resistors' values to 1 kΩ and select the closest available standard resistor values to produce gains of:

$$\begin{bmatrix} R_2 \\ R_3 \\ R_4 \\ R_5 \end{bmatrix} = \begin{bmatrix} 200 \\ 237 \\ 32.4 \\ 30.1 \end{bmatrix}. \quad R_1 = 1\ k\Omega. \quad GAINS = \begin{bmatrix} 3.002 \\ 5.007 \\ 23.99 \\ 49.82 \end{bmatrix}. \quad (13)$$

Figure 2 shows a parallel-resistor-ladder network. To select a gain value, connect an additional resistor in parallel with the other resistors. A circuit with N discrete gains requires N resistors in the ladder; an additional gain resistor, R_G; and N−1 switches. **Equation 14** describes the circuit's gain in the general case:

$$GAIN[n] = \frac{R_1 \| R_2 \| ... \| R_N}{R_G} + 1, \quad (14)$$

and **Equation 15** describes the parallel-resistor combination for each gain:

$$R_P[n] = (GAIN[n]-1) \times R_G. \quad (15)$$

The nth value of R_P equals the nth−1 value of R_P in parallel with the ladder's nth resistor. Solve the following equations for the nth resistor value:

$$R_P[n] = R_P[n-1] \| R_n, \quad (16)$$

$$R_1 = (GAIN[1]-1) \times R_G, \quad (17)$$

and

$$R_n = \frac{R_P[n] \times R_P[n-1]}{R_P[n-1]-R_P[n]}. \quad (18)$$

To find the desired network's resistors, select the desired gain values and R_G and then use **Equation 14** to calculate the parallel values. Use the resulting values to solve **Equation 15** and find the required resistor values. As in the previous example, a circuit must produce gain values of three, five, 24, and 50. Four gain values require four resistors. Let $R_G = 1\Omega$. Solving **Equation 14** for the parallel-values matrix yields:

$$\begin{bmatrix} R_P[1] \\ R_P[2] \\ R_P[3] \\ R_P[4] \end{bmatrix} = \begin{bmatrix} 49 \\ 23 \\ 4 \\ 2 \end{bmatrix}. \quad (19)$$

Substituting these values into **Equation 15** yields the resistors' values:

$$R_1 = 49 \times 1 = 49\Omega, \quad (20)$$

$$R_2 = \frac{23 \times 49}{49-23} = 43.35\Omega, \quad (21)$$

$$R_3 = \frac{4 \times 23}{23-4} = 4.842\Omega, \quad (22)$$

and

$$R_4 = \frac{2 \times 4}{4-2} = 4\Omega. \quad (23)$$

Scaling to 1 kΩ and selecting the closest available standard-value resistors yields gains of:

$$\begin{bmatrix} R_1 \\ R_2 \\ R_3 \\ R_4 \end{bmatrix} = \begin{bmatrix} 48{,}700 \\ 43{,}200 \\ 4870 \\ 4002 \end{bmatrix}. \quad R_G = 1\ k\Omega. \quad GAINS = \begin{bmatrix} 49.7 \\ 23.9 \\ 5.02 \\ 3 \end{bmatrix}. \quad (24)$$

Reference 1 provides a review of the matrix math. EDN

REFERENCE

1 Freeman, Larry, "Review of Matrices," Math Refresher, Dec 19, 2005, http://mathrefresher.blogspot.com/2005/12/review-of-matrices.html.

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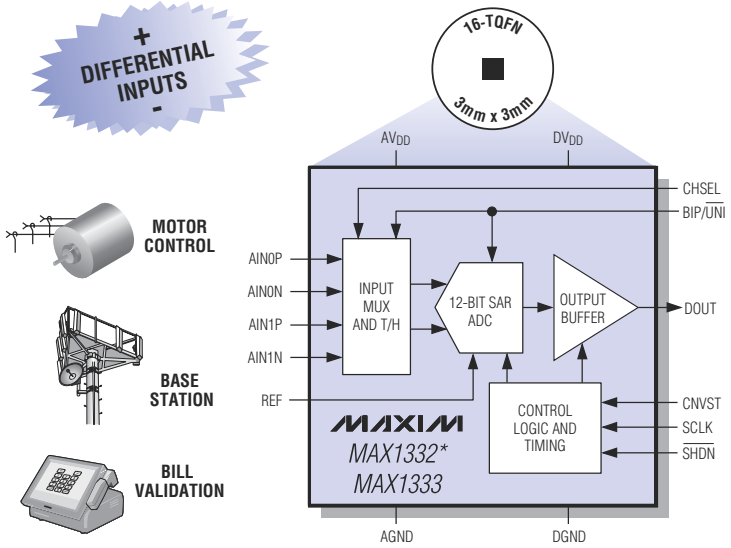

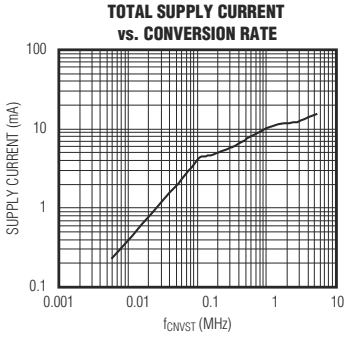

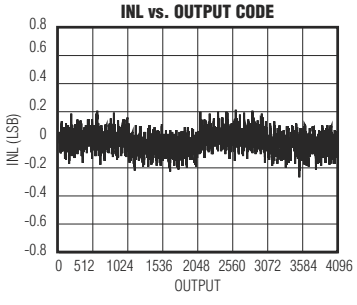

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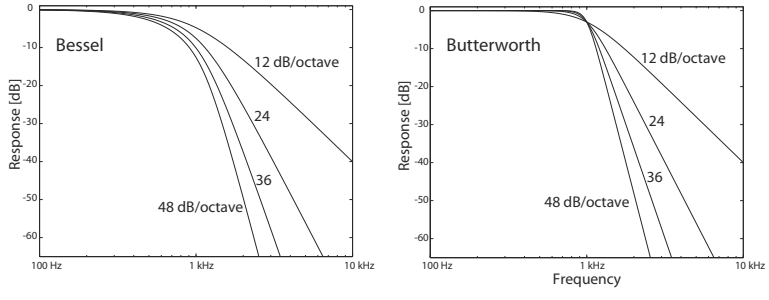

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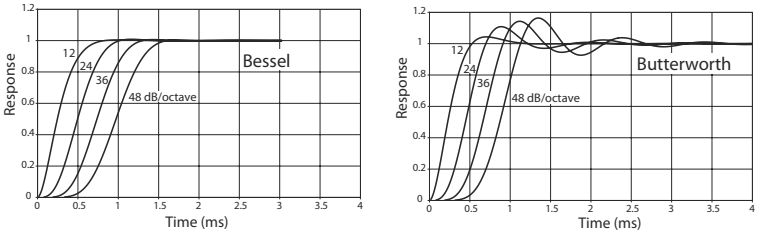

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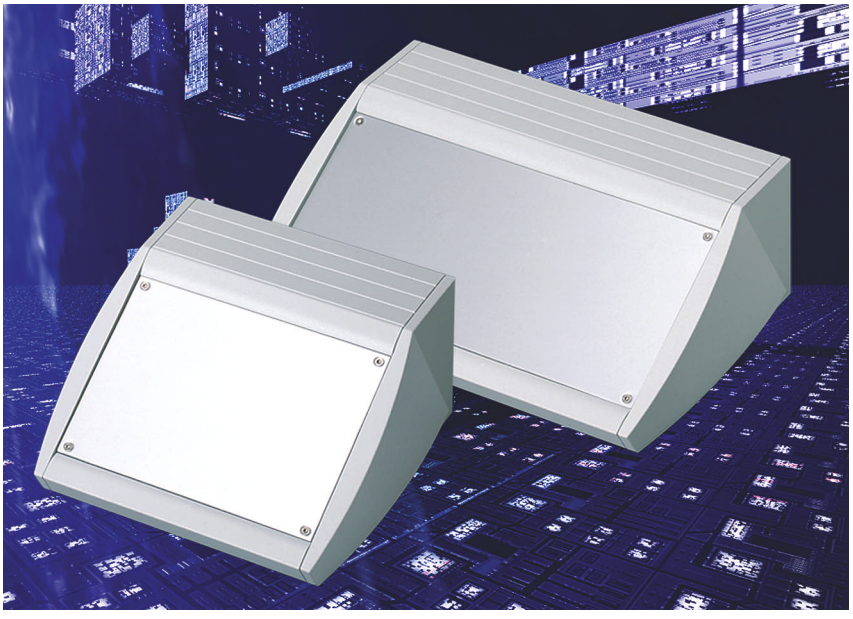

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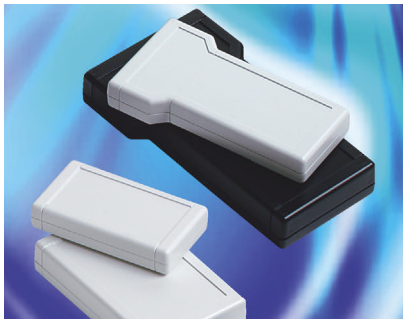

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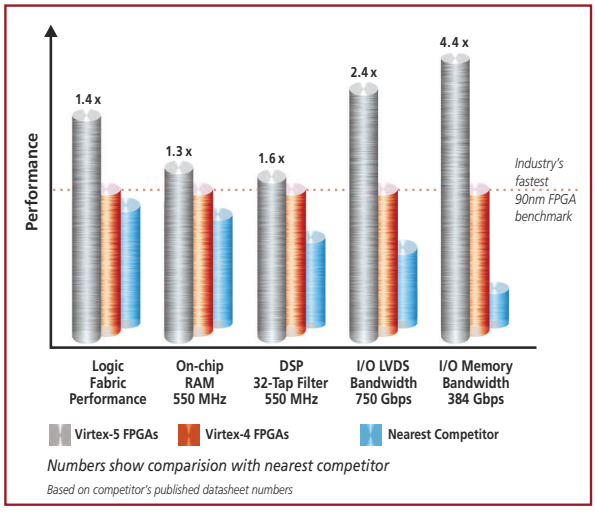

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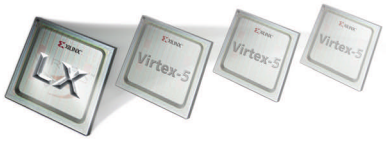

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6. **The Sony Reader paperback sized e-book**

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Entry details

All votes and entries to the prize-draw must be completed by August 14, 2006. One vote per individual and the prize-draw is not open to employees of Reed Business Information and Analog Devices.

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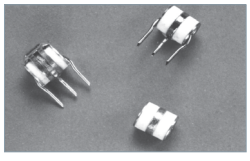

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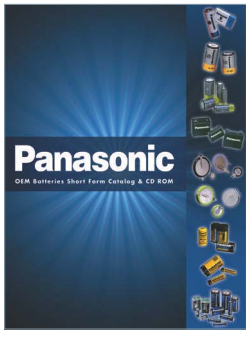

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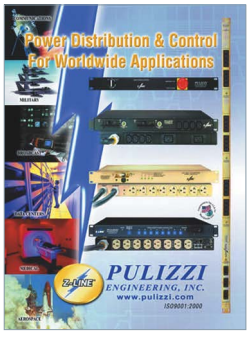

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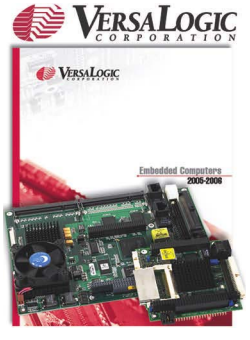

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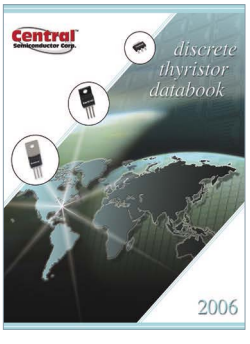

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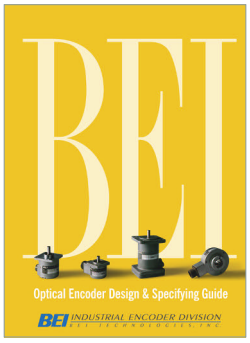

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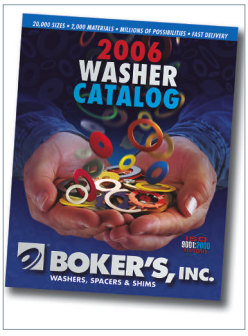

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STATS Total FSO venture funding: more than $300 million / 2006 market projection: $900 million

Free-space optics: last-mile link fogged in

Vendors have pushed approaches ranging from hovering airships (see www.edn.com/article/CA6339271) acting as wireless access points to massive mesh RF networks as the no-wires answer to last-mile links where no fiber exists. Several start-ups, meanwhile, focused on an optical approach—with no fiber optics required. The technology, FSO (free-space optics), relies on rooftop lasers and sensors to deliver high-speed point-to-point links between buildings. The target market includes both carrier-deployed services and enterprise-LAN connections between buildings, with data rates in excess of 1 Gbps.

Alas, San Diego-based LightPointe communications closed back in June—the last-standing FSO-focused business. Previously, AirFiber and Maxima Corp had exited the FSO business. Meanwhile, San Jose-based TeraBeam still offers some FSO products, although its primary focus is RF. A *San Diego Union Tribune* story on LightPointe's closing calculated the venture funding raised by the four at more than $300 million. Moreover, the story pointed out that early this decade, at least one analyst predicted a $900 million market by this year.

Unlike some failed technologies, FSO did find some success. Unfortunately for the FSO players, RF technologies such as Wi-Fi and emerging WiMax got cheap at the wrong time. Moreover, the line-of-sight requirement and real-word obstacles ranging from birds in flight to fog hobbled FSO.—by Maury Wright

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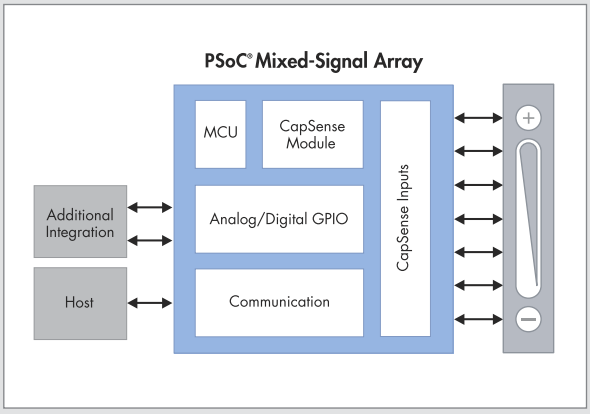

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